Ref. No. 4218
052010

ONKYO SERVICE MANUAL

BLU-RAY DISC PLAYER
MODEL BD-SP308(B)/(S)

RC-787DV /
RC-788DV

Black and Silver models

B WUP2P	200-240V AC, 50/60Hz
S WUP2P	200-240V AC, 50/60Hz
B WUL5P	200-240V AC, 50/60Hz
B WUF3N	110V AC, 60Hz
B WDC1N	120V AC, 60Hz
B WUQ3P	110-240V AC, 50/60Hz
B WUA4P	200-240V AC, 50/60Hz
B WUK3N	200-240V AC, 50/60Hz

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

ONKYO®
IMAGINATIVE SIGHT & SOUND

SCHEMATIC DIAGRAMS-1

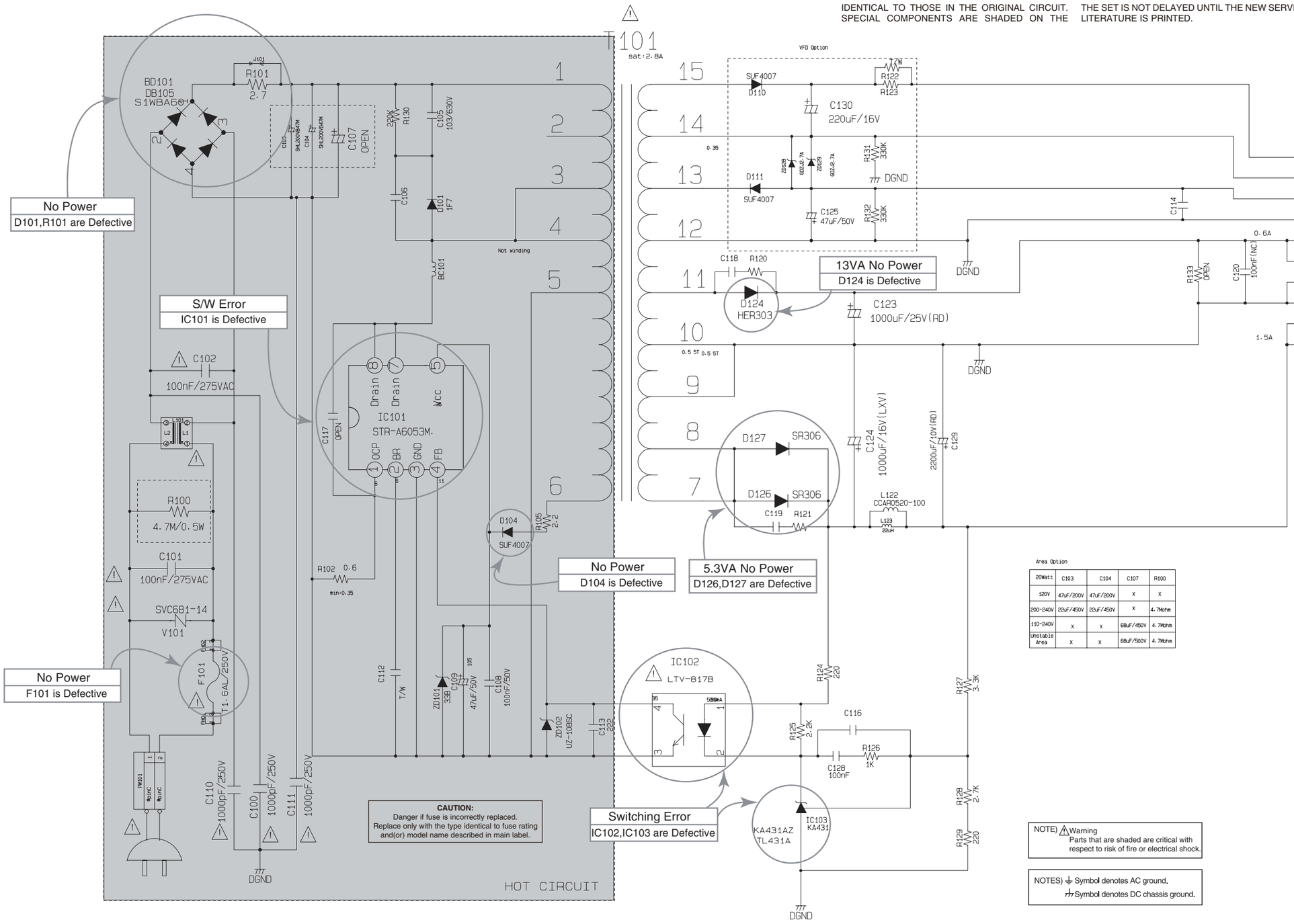
1. SMPS - POWER CIRCUIT

IMPORTANT SAFETY

WHEN SERVICING THIS CHASSIS, UNDER NO CIRCUMSTANCES SHOULD THE ORIGINAL DESIGN BE MODIFIED OR ALTERED WITHOUT PERMISSION FROM THE LG CORPORATION. ALL COMPONENTS SHOULD BE REPLACED ONLY WITH TYPES IDENTICAL TO THOSE IN THE ORIGINAL CIRCUIT. SPECIAL COMPONENTS ARE SHADED ON THE SCHEMATIC FOR EASY IDENTIFICATION. THIS CIRCUIT DIAGRAM MAY OCCASIONALLY DIFFER FROM THE ACTUAL CIRCUIT USED. THIS WAY, IMPLEMENTATION OF THE LATEST SAFETY AND PERFORMANCE IMPROVEMENT CHANGES INTO THE SET IS NOT DELAYED UNTIL THE NEW SERVICE LITERATURE IS PRINTED.

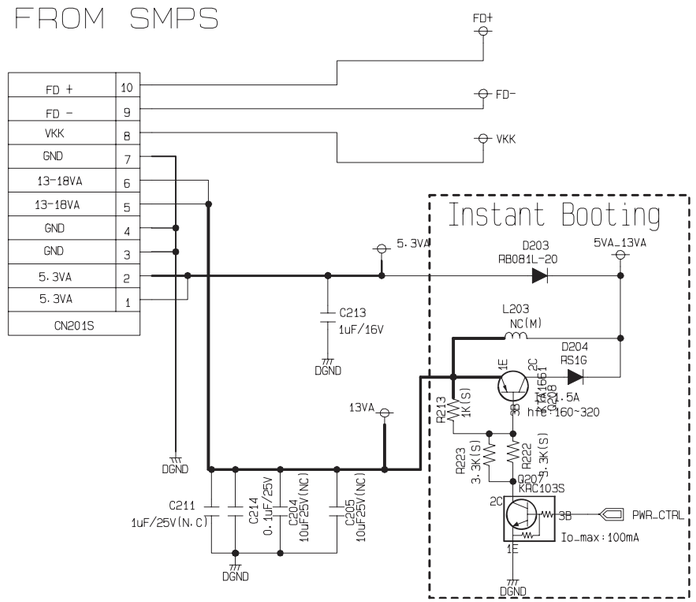
NOTE :

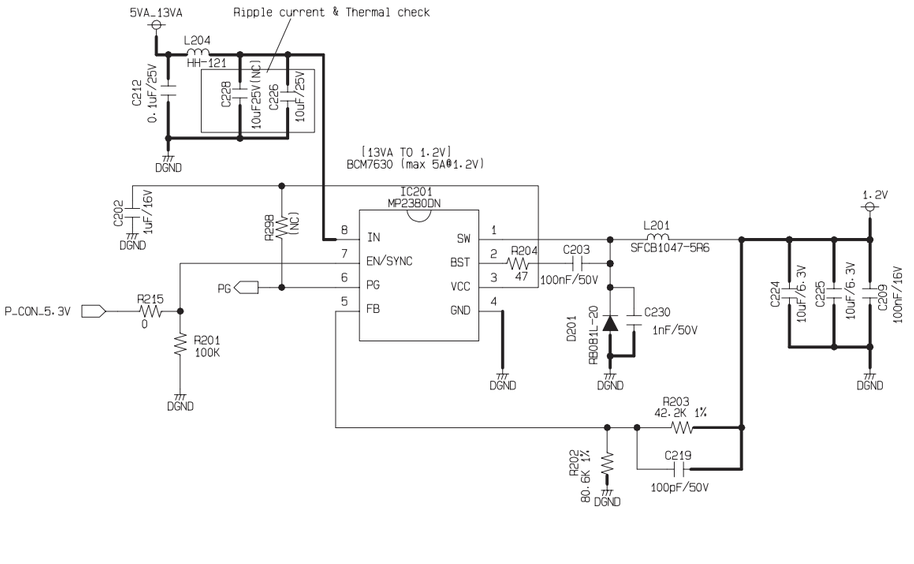
1. Shaded(▩) parts are critical for safety. Replace only with specified part number.
2. Voltages are DC-measured with a digital voltmeter during Play mode.

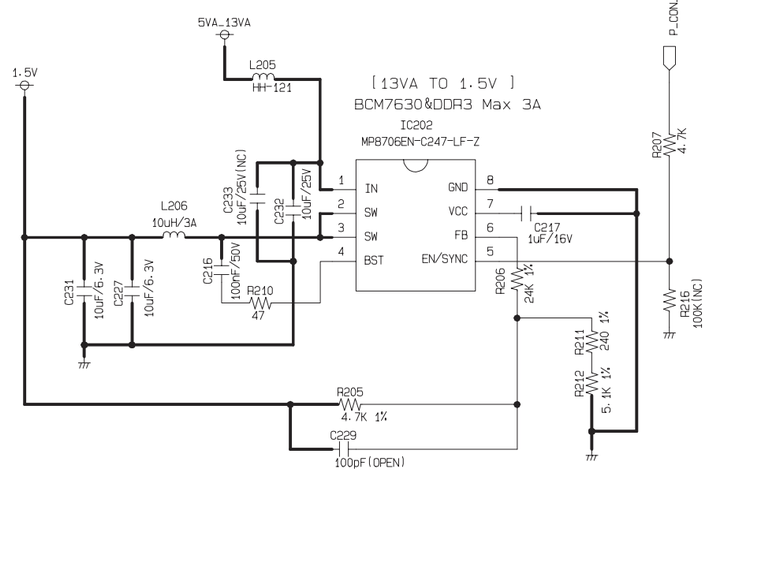


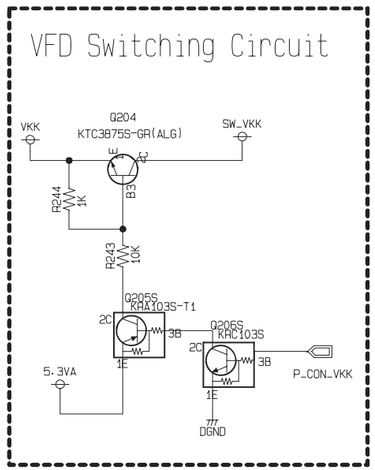
SCHEMATIC DIAGRAMS-2

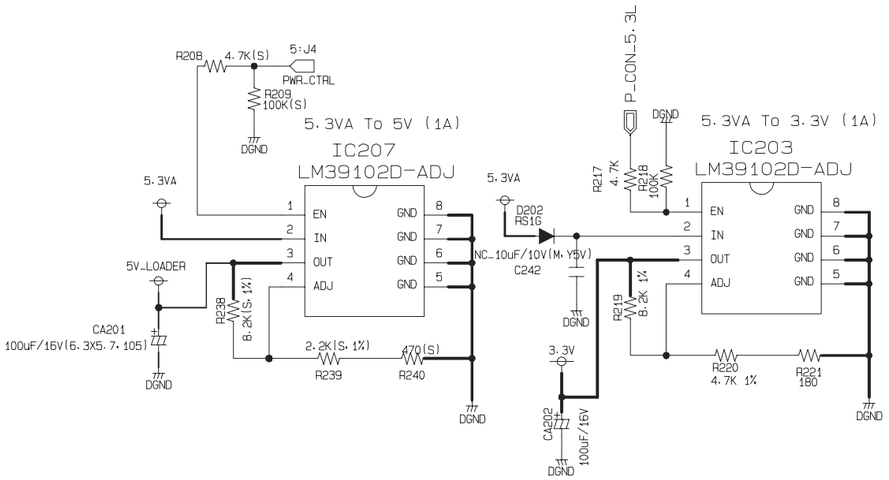
2. MAIN - MAIN POWER CIRCUIT

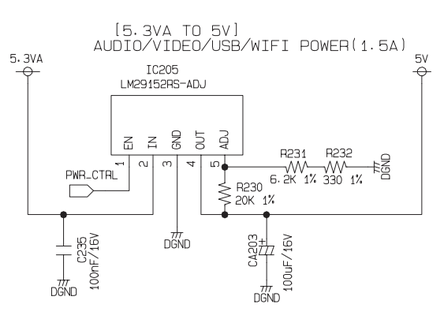


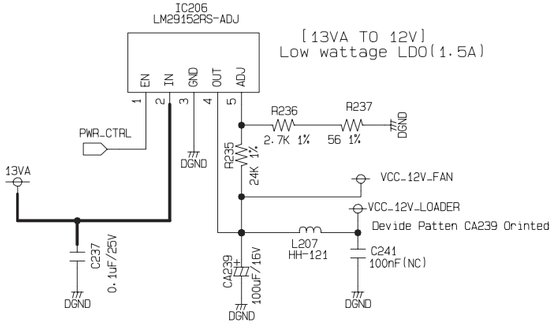






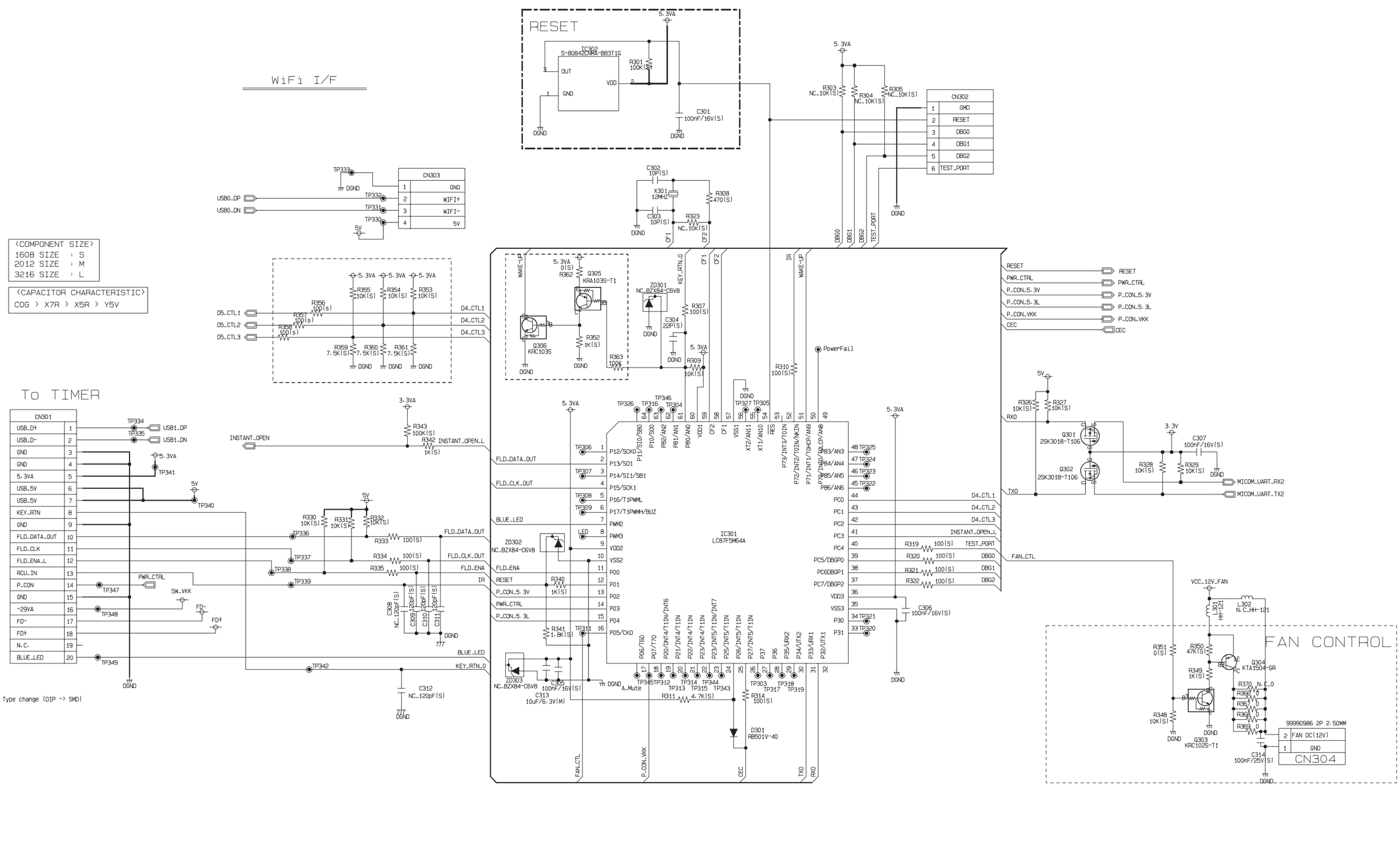






SCHEMATIC DIAGRAMS-3

3. MAIN - CPU 1 CIRCUIT

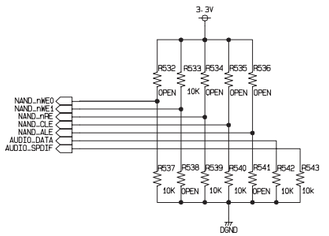


SCHEMATIC DIAGRAMS-4

4. MAIN - CPU 2 CIRCUIT

BCM7630 BOOT STRAP OPTIONS

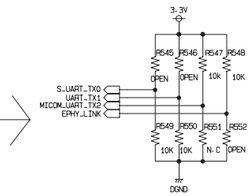
NO.	SIGNAL NAME	FIELD NAME	Description	VALUE
1	EBI_nWE0	STRAP_FLASH_WIDTH	NAND: 0=Allow writes to block 0. 1=Ignore writes to block 0	0
2	EBI_nWE1	STRAP_NAND_FLASH	1=NAND	1
3	NAND_nRE	STRAP_EBI_ROM_SIZE1	0 = No ECC 1 = 1 BIT ECC 2 = 4 BIT ECC 3 = 8 BIT ECC	1
4	NAND_CLE	STRAP_EBI_ROM_SIZE0		0
5	NAND_ALE	Reserved	-	-
6	I2S_SDATA	STRAP_SYSTEM_BIG_ENDIAN	0 = Little endian. 1=Big endian	0
7	BCM_SPDIF_OUT	STRAP_RESET_EXT_MODE	1 = Extend initial Reset	0

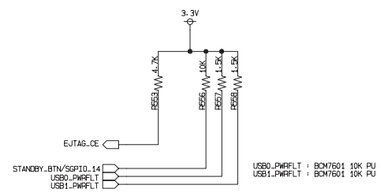


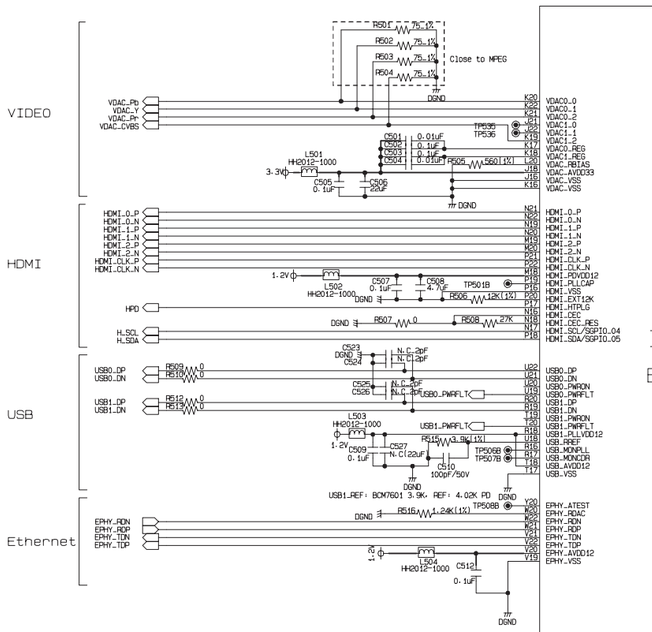
DDR STRAP OPTIONS

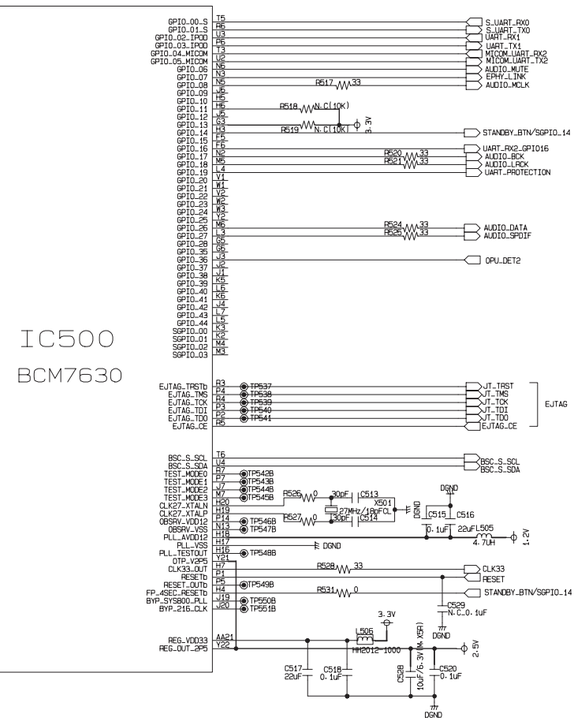
NO	SIGNAL NAME	VALUE
1	S_UART_TX0	1
2	IPOD_UART_TX1	0
3	UART_TX2	1
4	EPHY_LINK_GPIO07	0

These configuration resistors do not need to be close to the BCM7630.
So place them at the destination of the trace.

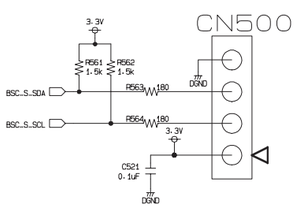




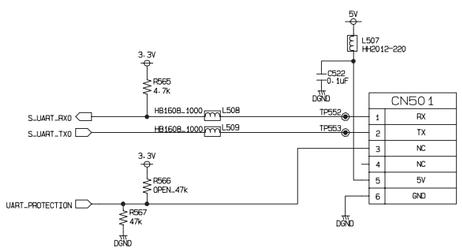


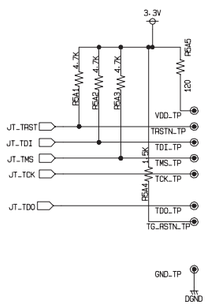


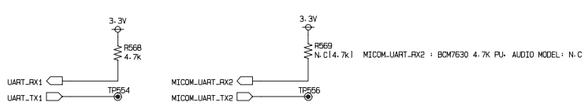
BBS I/F



DEBUGGING CONSOLE (UART1)

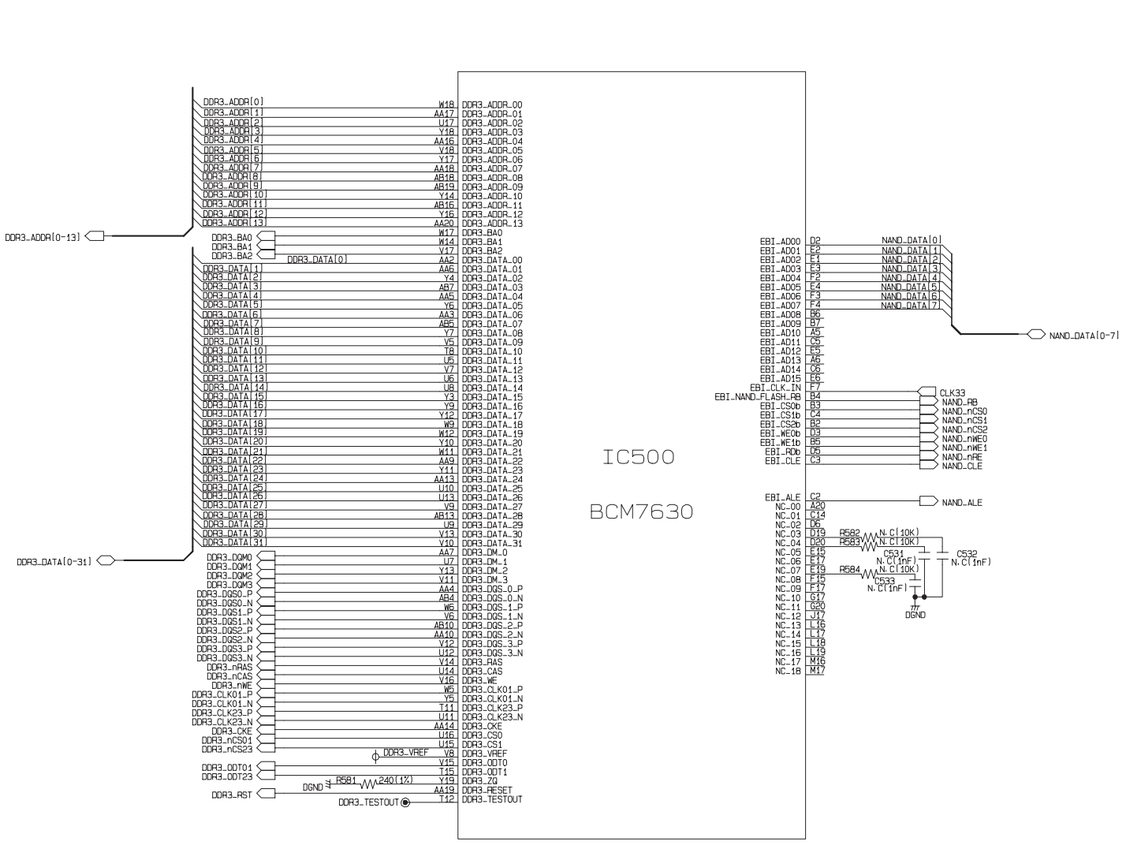


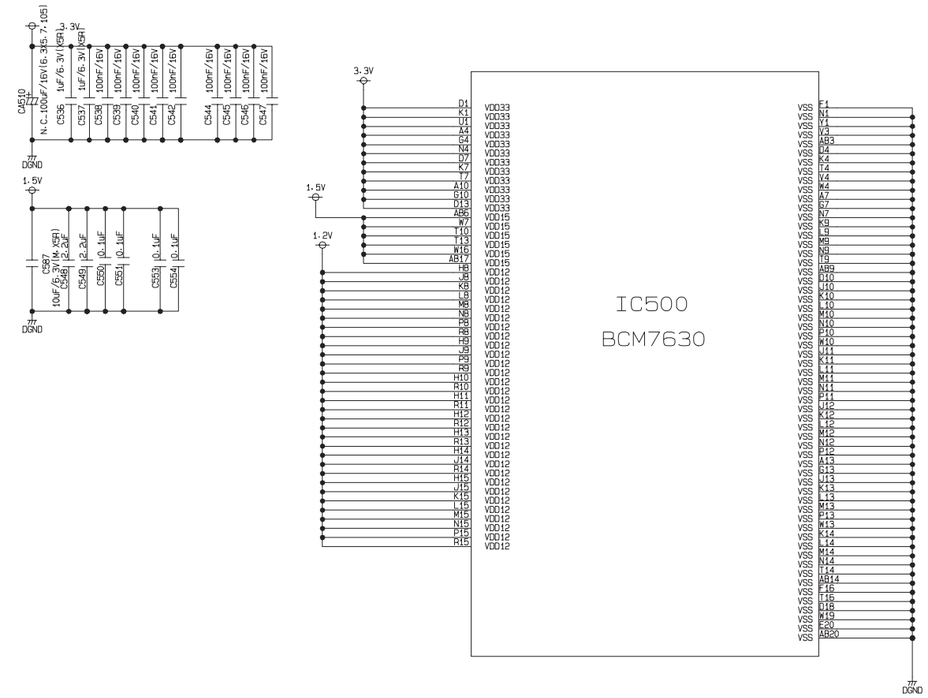


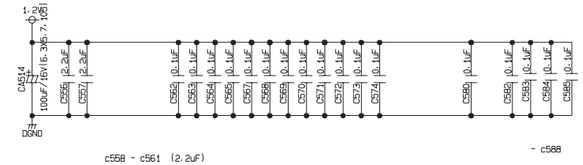


SCHEMATIC DIAGRAMS-5

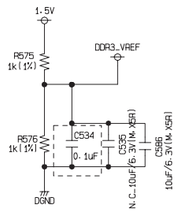
5. MAIN - CPU 3 CIRCUIT





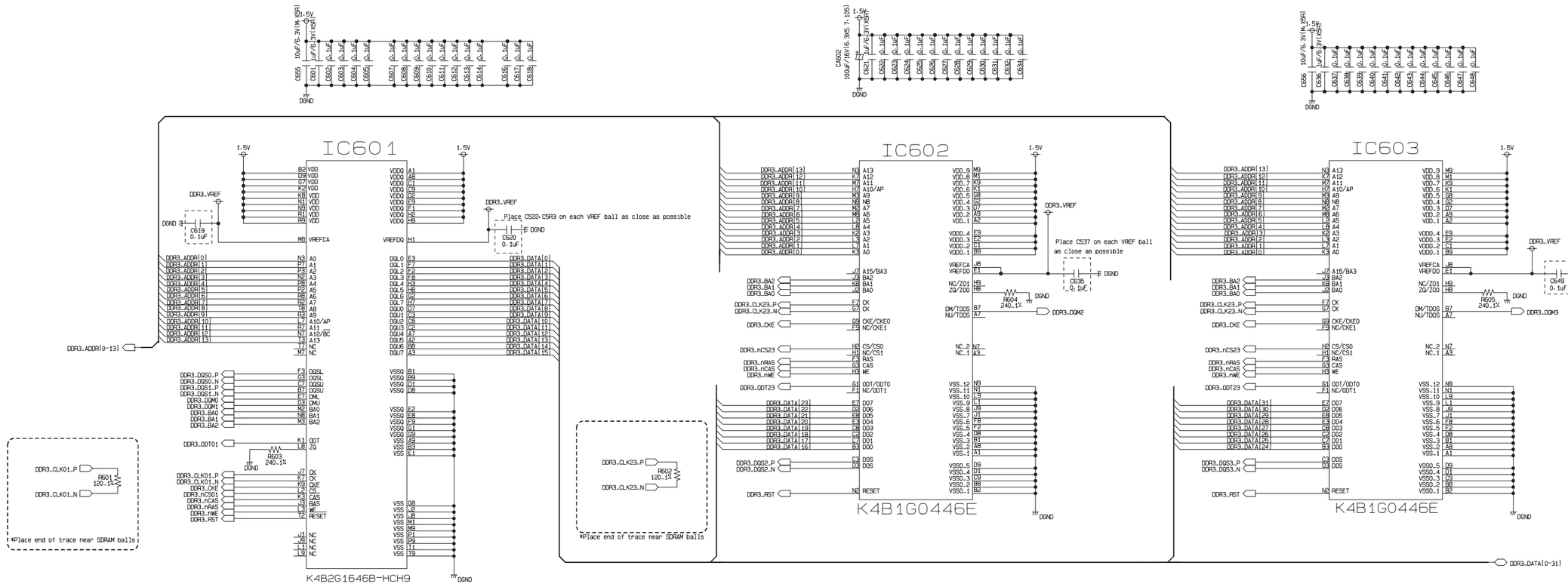


place C583 to V8 ball of 7630



SCHEMATIC DIAGRAMS-6

6. MAIN - DDR2, NAND, CP CIRCUIT



DDR3 : 512MB

DDR3 SDRAM LAYOUT GUIDE

* General Routing Guidelines

1. Do not route critical signals across split planes.
2. Route over appropriate 1.5V or ground plane.
3. Avoid routing memory signals closer than 25-mil to the memory clocks.
4. DDR Clock and DQS routed differentially (120ohm)
5. Use proper 120ohm clock termination
6. Vref decoupling close to DRAM
7. Vref decoupling close to ASIC
8. VDD/VDDQ decoupling close to DRAM VDD/VDDQ pins
9. VDDQ decoupling close to ASIC VDDQ pins

* Clock Routing Guidelines

10. Clocks must maintain length matching between clock pairs of 25 mils.
11. Differential clocks need to maintain length matching between positive and negative signals of 15 mils routed in parallel.
12. The space between differential pairs must be at least 2 the trace width of the differential pair to minimize loss and maximize interconnect density.
13. Match DQS signal length to related Clock signal length to within 475 mils

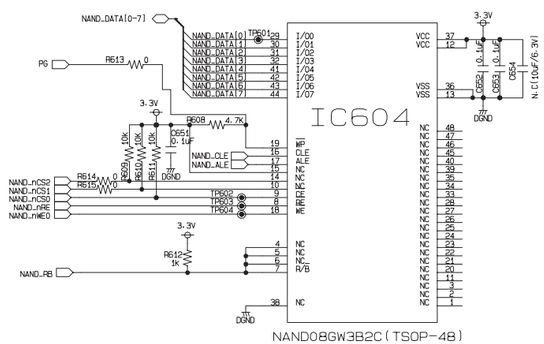
* Address and Command Routing Guidelines

14. Address and command signals are routed in a daisy chain topology from the first SDRAM to the last SDRAM.
15. Ensure that each net maintains the same consecutive order.
16. Do not route differential clock and clock enable signals close to address signals.
17. Route all addresses and commands to match related clock signals to within 475 mils to each discrete memory component.
(Values apply for two loads when both are near the end of the wire and the wire is not terminated. The Address/Control wire length to the first load should be longer than the clock wires.)

* DQ- DQS- and DM Routing Guidelines

18. All signals within a given Byte Lane Group must be matched in length with a maximum deviation of 250mils.
19. Route all DQS- DQM signals to match related DQ byte lane signals to within 250 mils

SLC NAND : 256MB

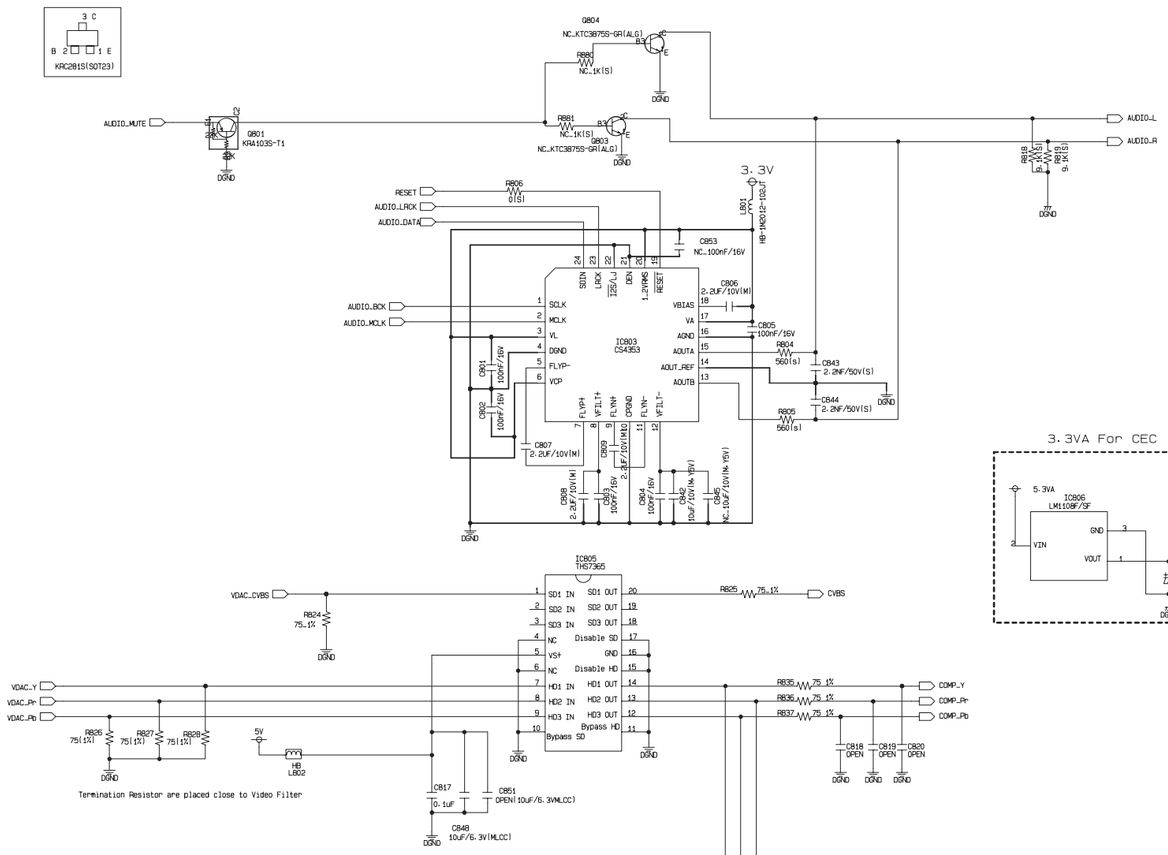


SCHEMATIC DIAGRAMS-7

7. MAIN - BCM7630 FRONT END CIRCUIT

SCHEMATIC DIAGRAMS-8

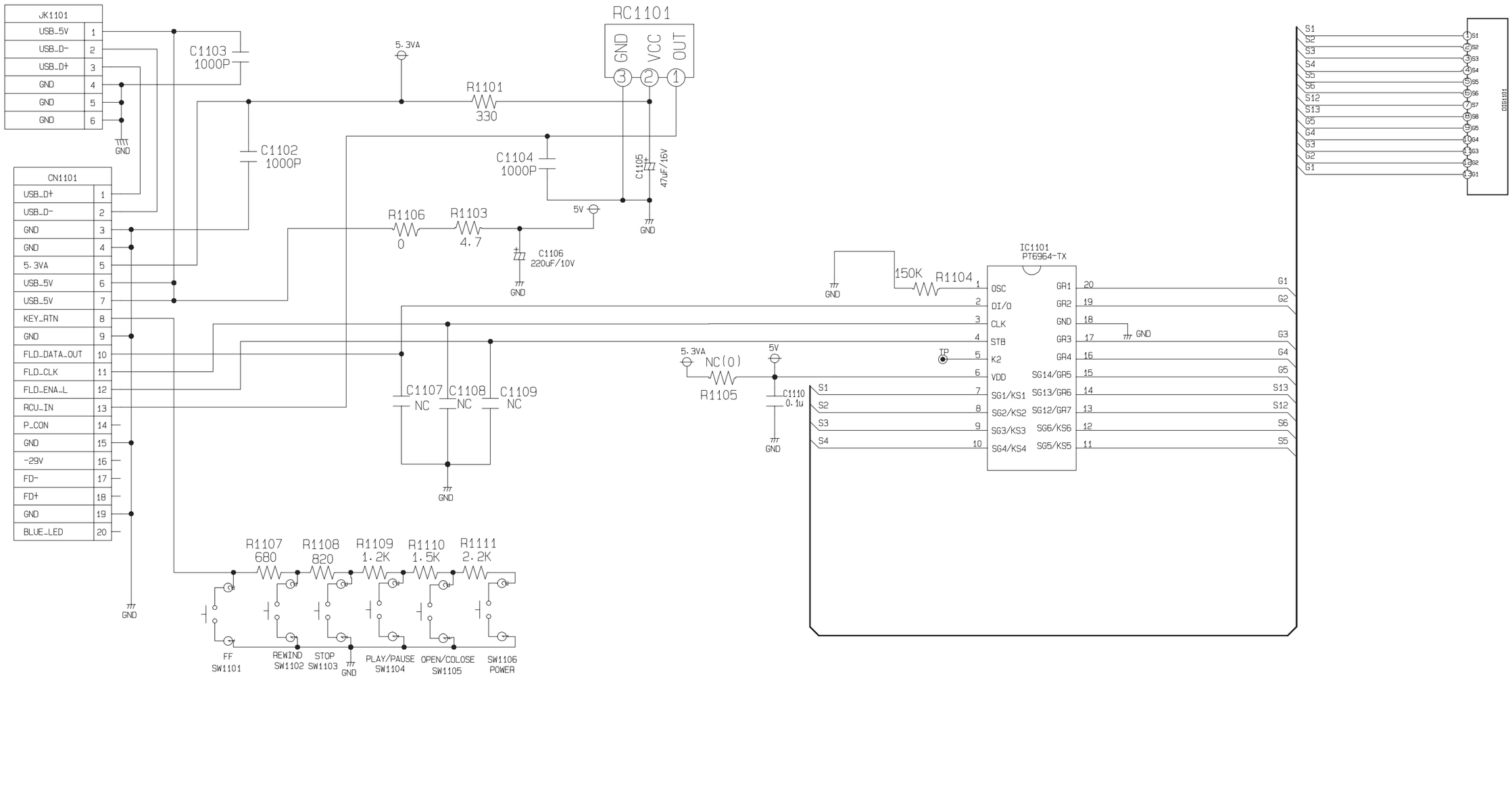
8. MAIN - AUDIO/VIDEO OUTPUT CIRCUIT



SCHEMATIC DIAGRAMS-9

9. FRONT - TIMER CIRCUIT

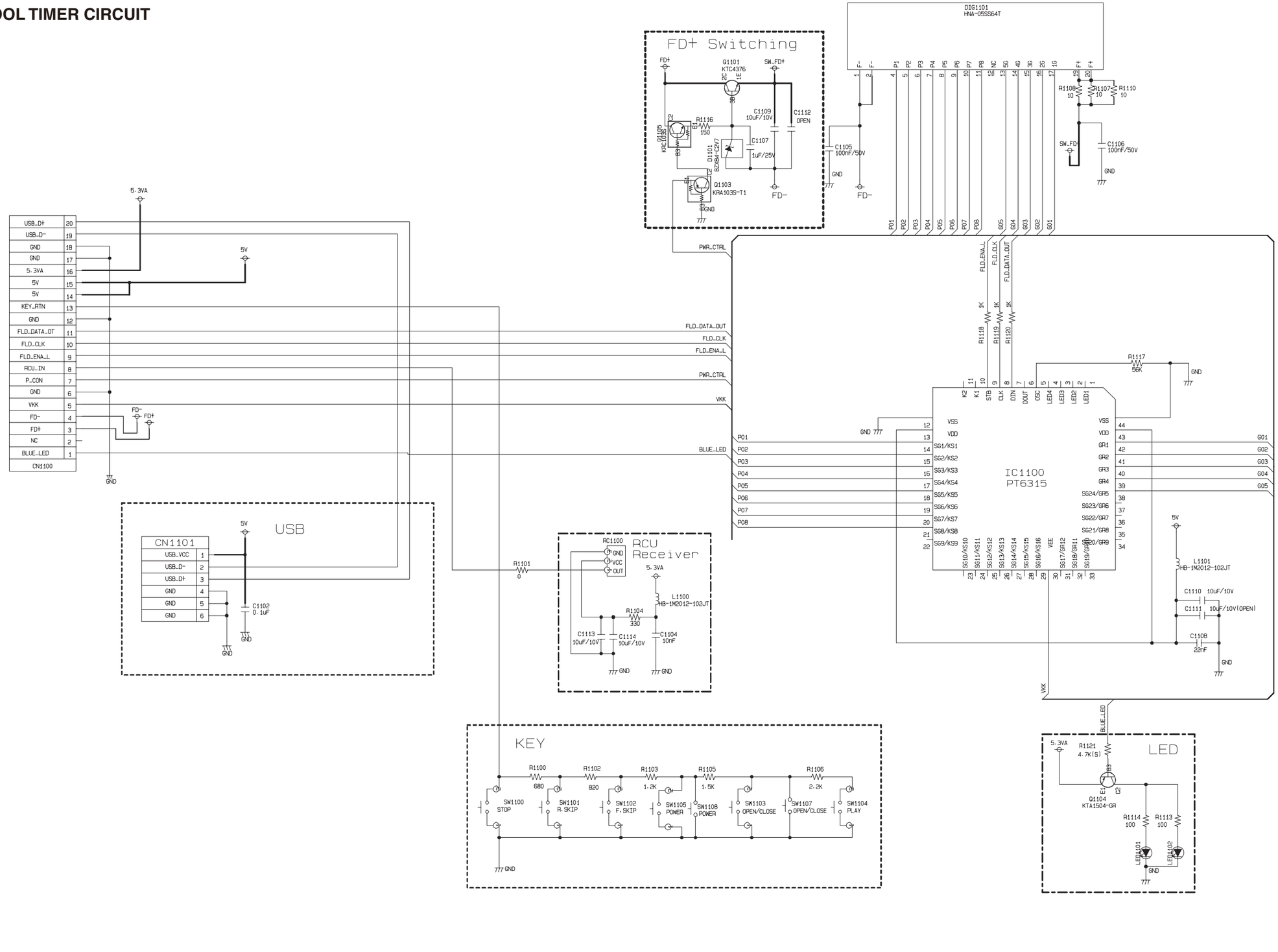
9-1. TOOL TIMER CIRCUIT



SCHEMATIC DIAGRAMS-10

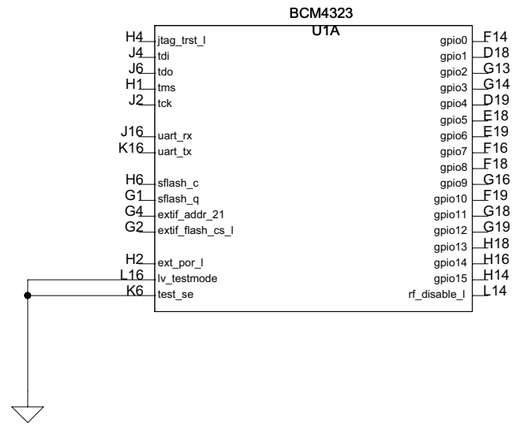
9. FRONT - TIMER CIRCUIT

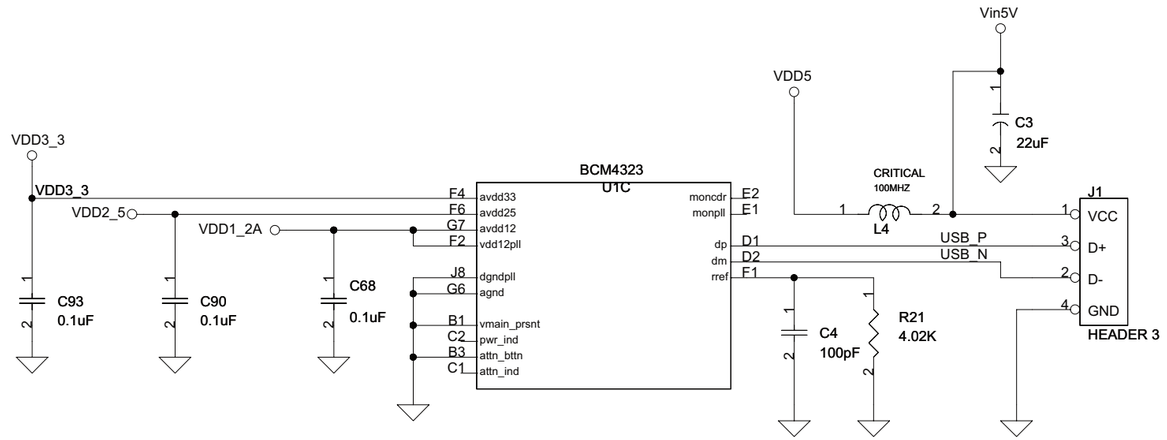
9-2. TOOL TIMER CIRCUIT

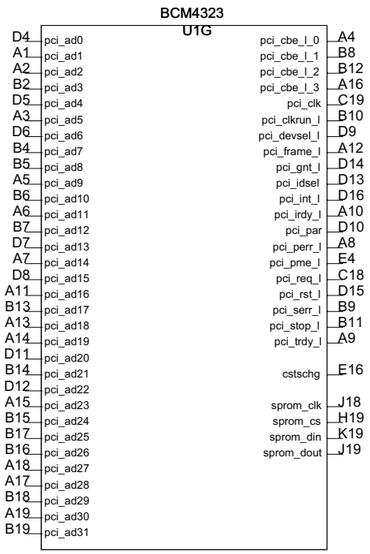


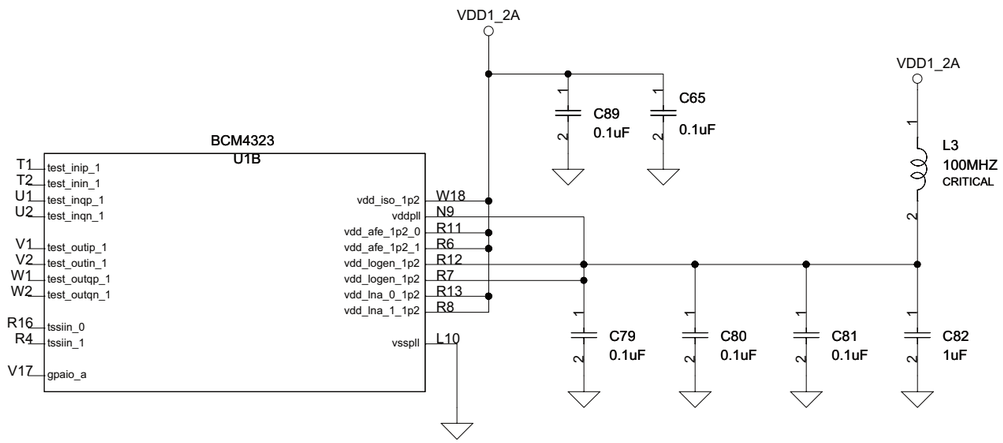
SCHEMATIC DIAGRAMS-11

10. WiFi - USB GPIO STRAP CIRCUIT





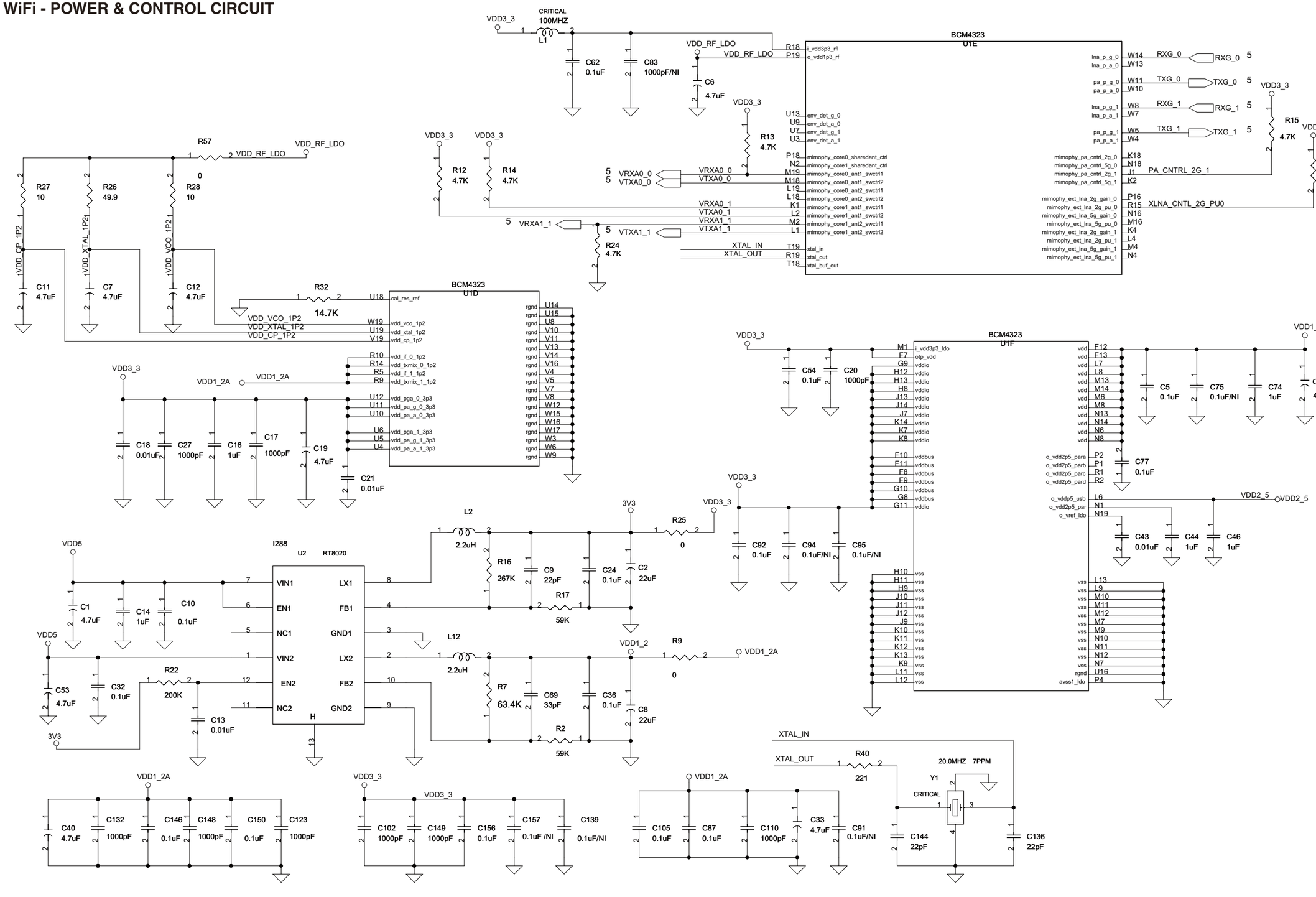




Pin name	Netname	Status
mimophy_core1_ant2_swctrl_1	VRXA1_1	ext PD
mimophy_core1_ant1_swctrl_1	VRXA0_1	ext PU
mimophy_pa_cntrl_2g_1	PA_cntrl_2G_1	ext PU
mimophy_core0_ant1_swctrl_1	VRXA0_0	ext PU
mimophy_ext_lna_2g_pu_0	xlna_cntl_2g_pu0	ext PU
mimophy_core1_ant1_swctrl_2	VTXA0_1	ext PU

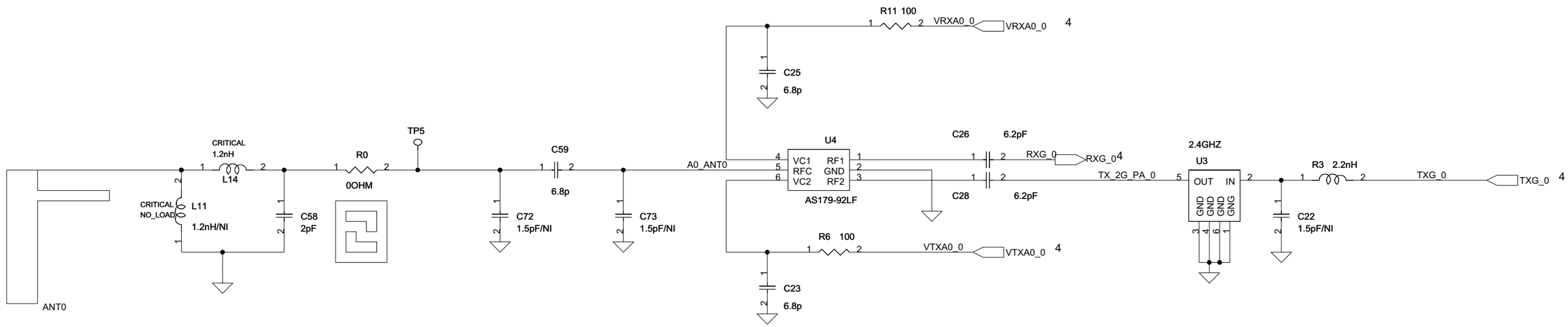
SCHEMATIC DIAGRAMS-12

11. WiFi - POWER & CONTROL CIRCUIT



SCHEMATIC DIAGRAMS-13

12. WiFi - RF ANTENNA CIRCUIT



SCHEMATIC DIAGRAMS-14

CIRCUIT VOLTAGE CHART

1. MAIN BOARD - ICs

PIN NO.	DESCRIPTION	VOLTAGE	
		PLAY MODE	NO PLAY MODE
IC201(MP2377)			
1	Vout	1.22	1.22
8	Vin	12.47	12.35
IC202(MP8706)			
1	Vin	12.47	12.36
3	Vout	1.51	1.51
IC203(LM39102D)			
2	Vin	4.45	4.47
3	Vout	3.33	3.33
IC205(LM29152)			
2	Vin	5.35	5.36
4	Vout	5	5.01
IC206(LM29152)			
2	Vin	13.43	13.32
4	Vout	12.12	12.13
IC207(LM39102D)			
1	Vin	5.35	5.36
2	Vout	4.98	4.99
IC803(CS4353) DAC+AMP			
3	VL	3.329V	3.337V
6	VCP	3.329V	3.337V
18	VA	3.329V	3.337V
20	V_2VRMS	3.329V	3.337V
IC805 Video Amp			
5	VCC	5.07	
20	CVBS Out	1.64	

2. MAIN BOARD - Capacitors

LOCA. NO.	CAPACITY	PLAY MODE		NO PLAY MODE	
		POSITIVE	NEGATIVE	POSITIVE	NEGATIVE
CA201	100uF/16V	4.98	0	4.98	0
CA202	100uF/16V	3.33	0	3.33	0
CA203	100uF/16V	5	0	5.01	0
CA239	100uF/16V	12.12	0	12.12	0
CA514	100uF/16V	1.21	0	1.21	0
CA602	100uF/16V	1.51	0	1.51	0
CA805	100uF/16V	3.3	0	3.3	0

3. FRONT BOARD

PIN NO.	DESCRIPTION	VOLTAGE
DIG1101(HNS-05SS64T)		
FD+	-	-18.9
FD-	-	-20.6
IC1100(PT6315) VFD Driver IC		
13, 43	VDD	4.99
30	VKK	-23.01
Q1101(KTC4375)		
Emitter	-	-18.9
Base	-	-18.01
Collector	-	-16.9
Q1105(KRC103S)		
Emitter	-	-16.86
Base	-	4.93
Collector	-	-16.89
Q1103(KRA103S)		
Emitter	-	4.96
Base	-	0
Collector	-	4.93
RC1100 RCU Receiver		
2	VCC	5.01

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ONKYO
HOMEPAGE
http://www.onkyo.com/