

ONKYO SERVICE MANUAL

BLU-RAY DISC PLAYER MODEL BD-SP308(B)/(S)

RC-787DV /
RC-788DV

Black and Silver models

B WUP2P	200-240V AC, 50/60Hz
S WUP2P	200-240V AC, 50/60Hz
B WUL5P	200-240V AC, 50/60Hz
B WUF3N	110V AC, 60Hz
B WDC1N	120V AC, 60Hz
B WUQ3P	110-240V AC, 50/60Hz
B WUA4P	200-240V AC, 50/60Hz
B WUK3N	200-240V AC, 50/60Hz

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK \triangle ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

SCHEMATIC DIAGRAMS-1

1. SMPS - POWER CIRCUIT

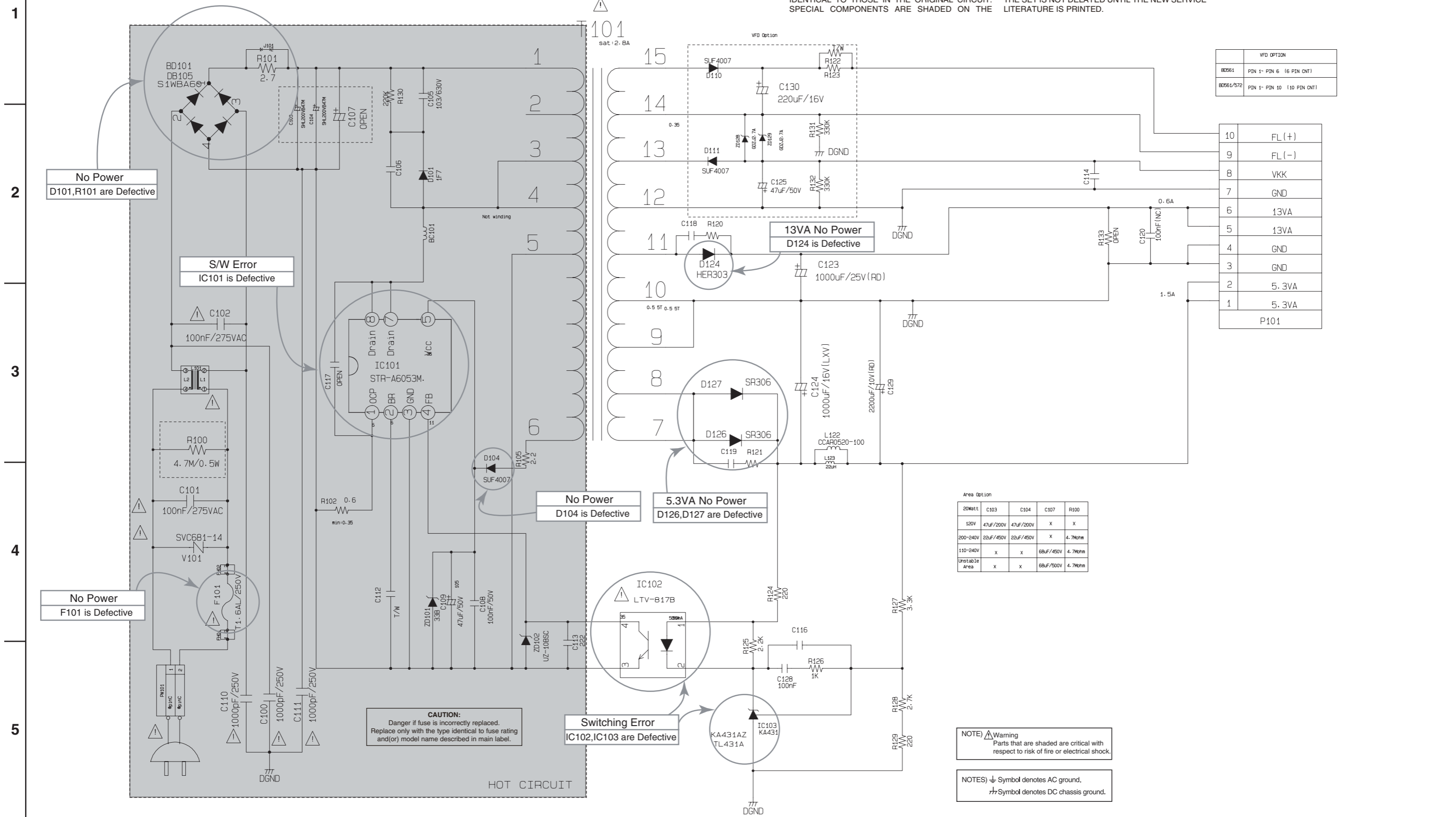
IMPORTANT SAFETY

WHEN SERVICING THIS CHASSIS, UNDER NO CIRCUMSTANCES SHOULD THE ORIGINAL DESIGN BE MODIFIED OR ALTERED WITHOUT PERMISSION FROM THE LG CORPORATION. ALL COMPONENTS SHOULD BE REPLACED ONLY WITH TYPES IDENTICAL TO THOSE IN THE ORIGINAL CIRCUIT. SPECIAL COMPONENTS ARE SHADED ON THE

SCHEMATIC FOR EASY IDENTIFICATION. THIS CIRCUIT DIAGRAM MAY OCCASIONALLY DIFFER FROM THE ACTUAL CIRCUIT USED. THIS WAY, IMPLEMENTATION OF THE LATEST SAFETY AND PERFORMANCE IMPROVEMENT CHANGES INTO THE SET IS NOT DELAYED UNTIL THE NEW SERVICE LITERATURE IS PRINTED.

NOTE :

1. Shaded(■) parts are critical for safety. Replace only with specified part number.
2. Voltages are DC-measured with a digital voltmeter during Play mode.



No Power
D101,R101 are Defective

S/W Error
IC101 is Defective

No Power
F101 is Defective

No Power
D104 is Defective

5.3VA No Power
D126,D127 are Defective

Switching Error
IC102,IC103 are Defective

13VA No Power
D124 is Defective

CAUTION:
Danger if fuse is incorrectly replaced.
Replace only with the type identical to fuse rating and/or model name described in main label.

VFD OPTION	
BC561	PIN 1- PIN 6 (6 PIN CNT)
BC561/572	PIN 1- PIN 10 (10 PIN CNT)

10	FL(+)
9	FL(-)
8	VKK
7	GND
6	13VA
5	13VA
4	GND
3	GND
2	5.3VA
1	5.3VA
P101	

Area Option

20Watt	C103	C104	C107	R100
120V	47uF/200V	47uF/200V	X	X
200-240V	22uF/450V	22uF/450V	X	4.7Mohm
110-240V	X	X	68uF/450V	4.7Mohm
Unstable Area	X	X	68uF/500V	4.7Mohm

NOTE) ⚠ Warning
Parts that are shaded are critical with respect to risk of fire or electrical shock.

NOTES) ⊥ Symbol denotes AC ground.
⏏ Symbol denotes DC chassis ground.

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101
sat: 2-BA

HOT CIRCUIT

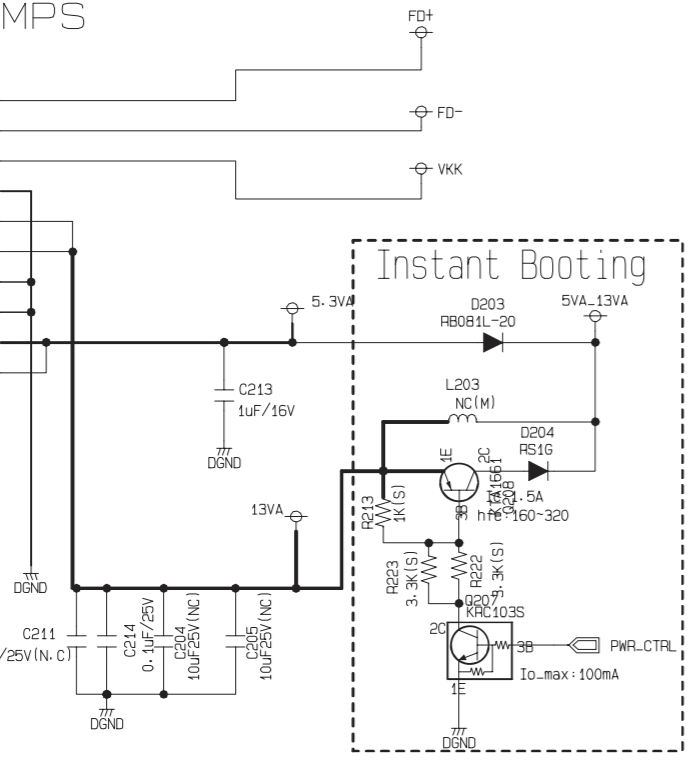
SCHEMATIC DIAGRAMS-2

2. MAIN - MAIN POWER CIRCUIT

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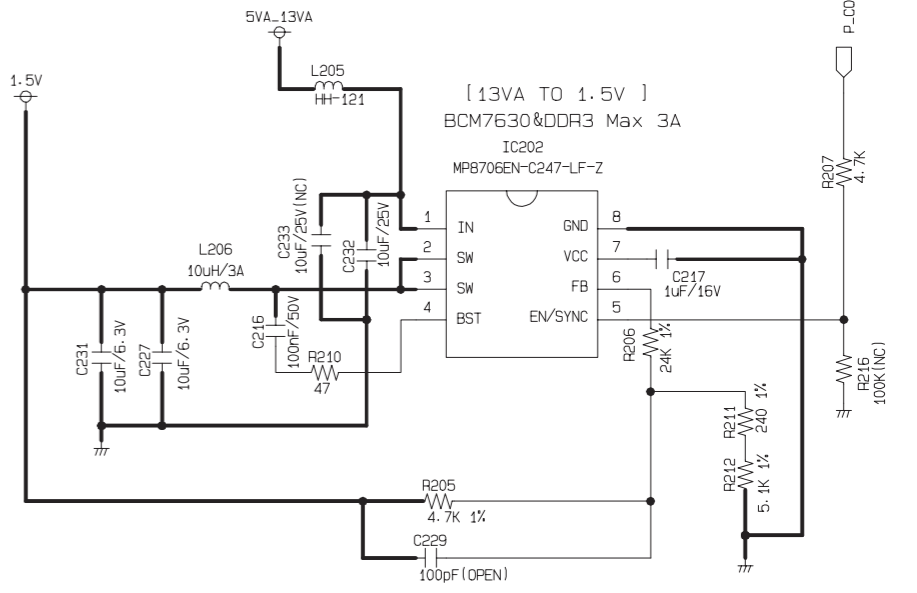
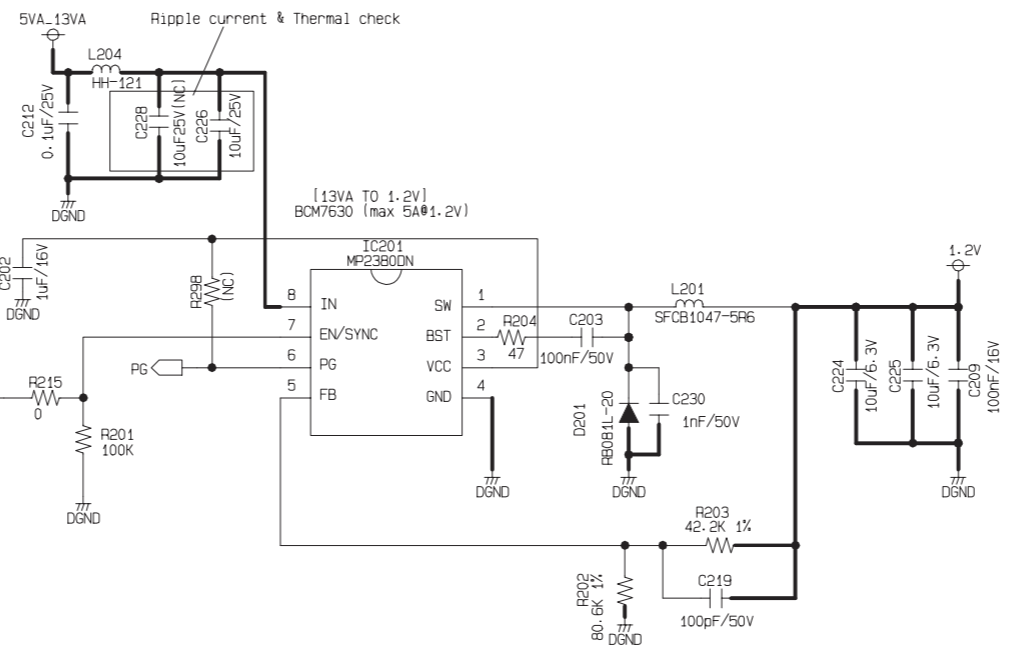
FROM SMPS

FD +	10
FD -	9
VKK	8
GND	7
13-18VA	6
13-18VA	5
GND	4
GND	3
5.3VA	2
5.3VA	1
CN201S	



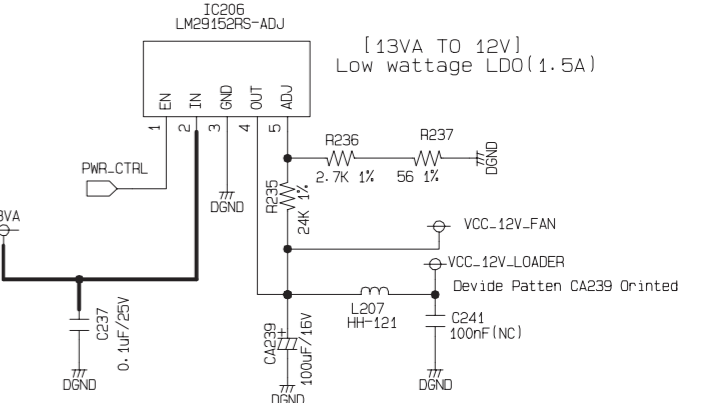
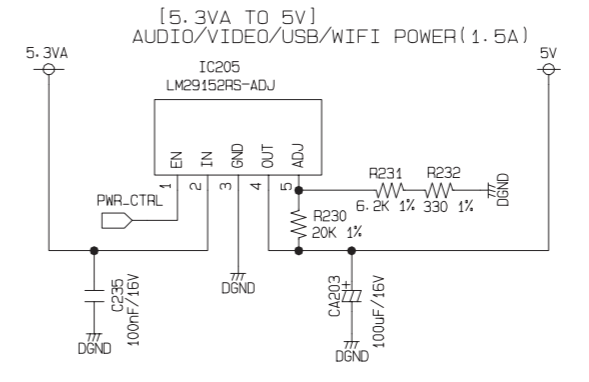
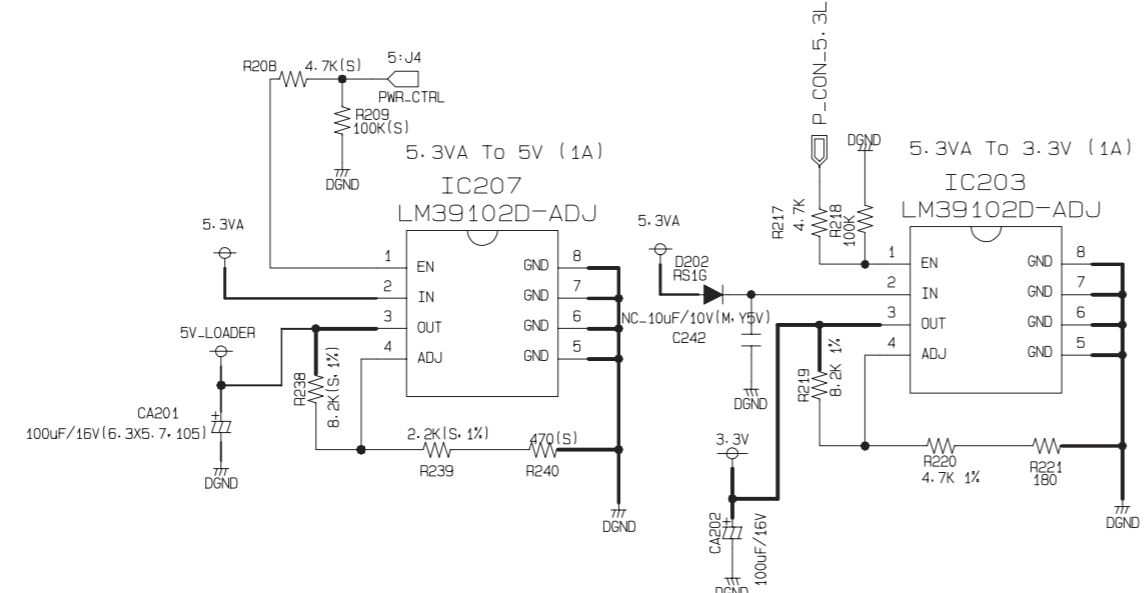
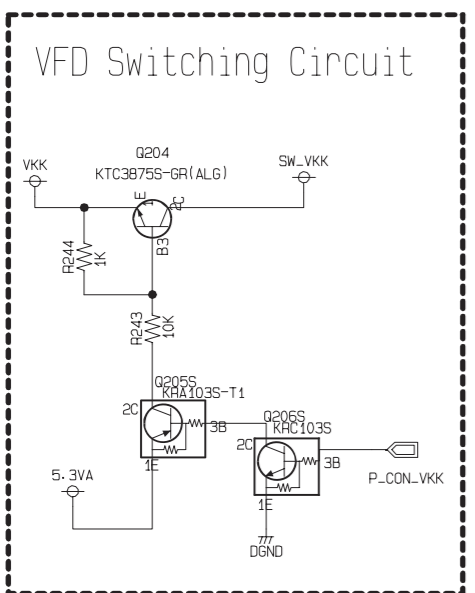
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SCHEMATIC DIAGRAMS-3

3. MAIN - CPU 1 CIRCUIT

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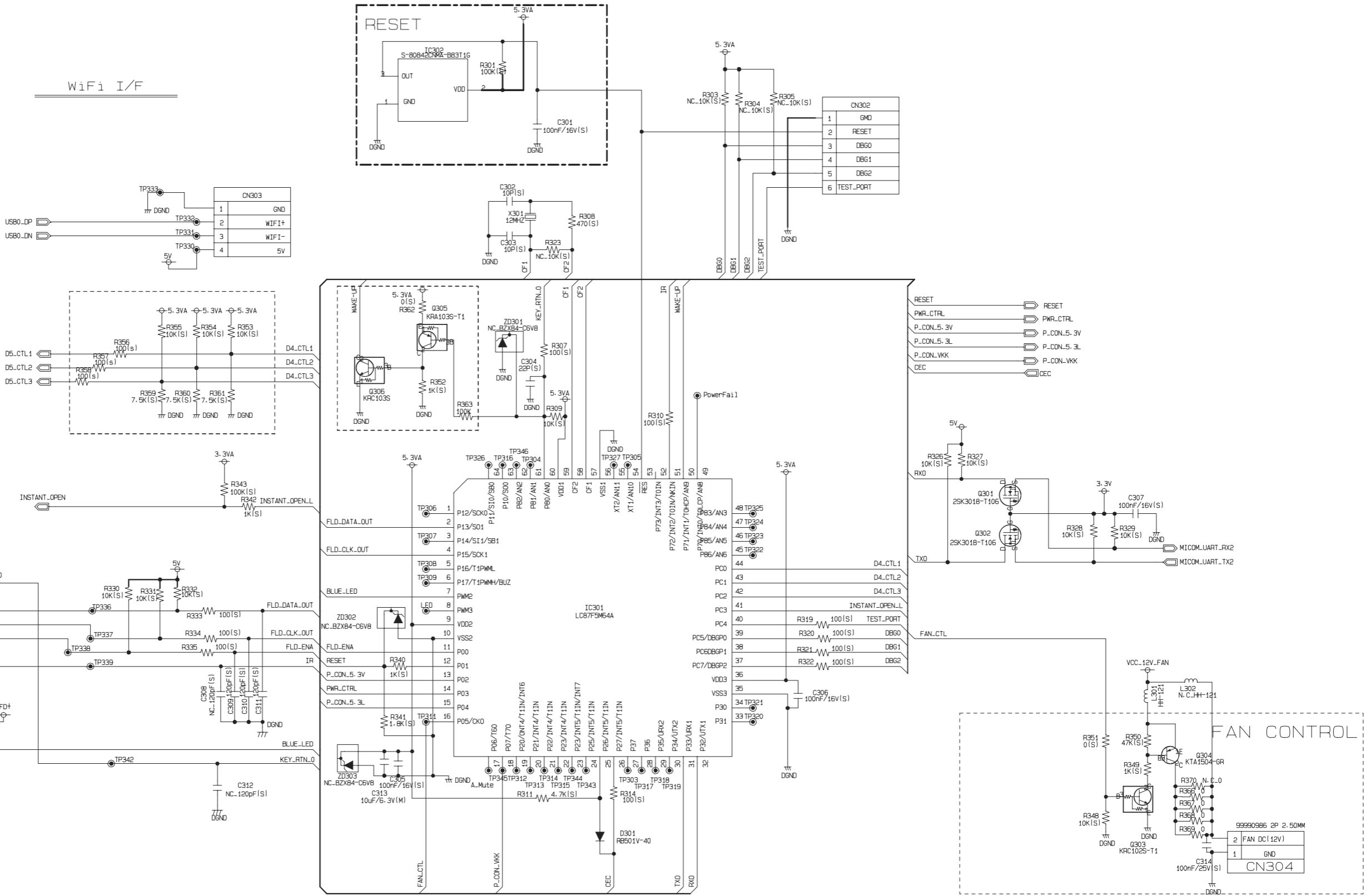
<COMPONENT SIZE>
 1608 SIZE : S
 2012 SIZE : M
 3216 SIZE : L

<CAPACITOR CHARACTERISTIC>
 COG > X7R > X5R > Y5V

To TIMER

CN301	
1	USB_DP
2	USB_DN
3	GND
4	GND
5	5.3VA
6	USB_5V
7	USB_5V
8	KEY_RTN
9	GND
10	FLD_DATA_OUT
11	FLD_CLK
12	FLD_ENA.L
13	RCU_IN
14	P_CON
15	GND
16	-29VA
17	FD-
18	FD+
19	N.C.
20	BLUE_LED

Type change (DIP -> SMD)



CN302	
1	GND
2	RESET
3	DBG0
4	DBG1
5	DBG2
6	TEST_PORT

CN303	
1	GND
2	WiFi+
3	WiFi-
4	5V

RESET	RESET
PWR_CTRL	PWR_CTRL
P_CON.5_3V	P_CON.5_3V
P_CON.5_3L	P_CON.5_3L
P_CON.VKK	P_CON.VKK
CEC	CEC

CN304	
1	GND
2	FAN DC(12V)

SCHEMATIC DIAGRAMS-4

4. MAIN - CPU 2 CIRCUIT

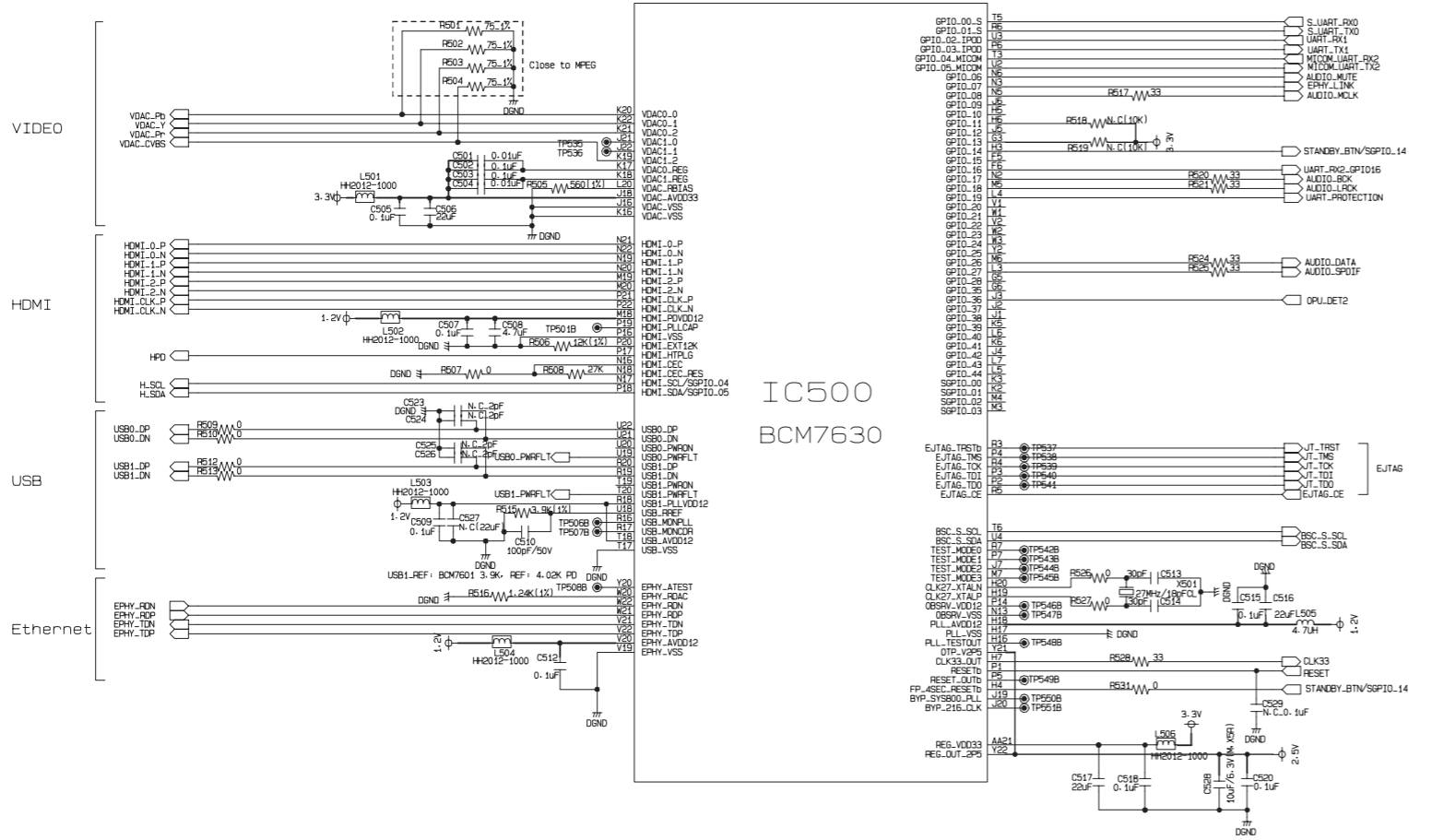
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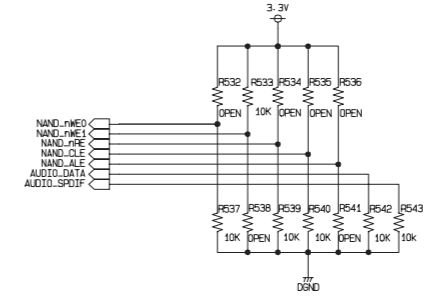
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BCM7630 BOOT STRAP OPTIONS

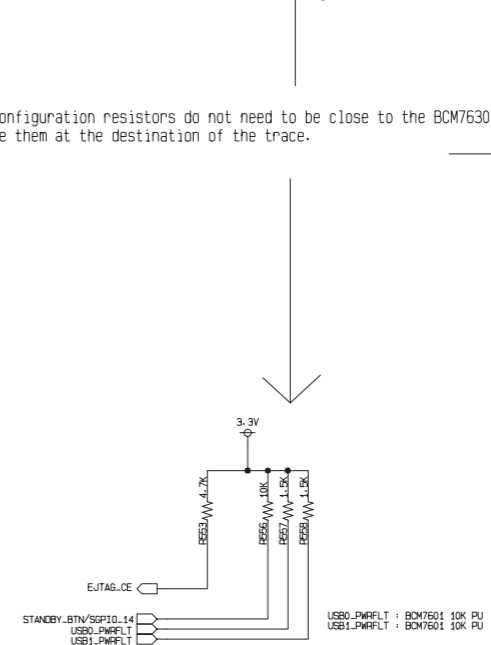
NO.	SIGNAL NAME	FIELD NAME	Description	VALUE
1	EBI_nWE0	STRAP_FLASH_WIDTH	NAND: 0=Allow writes to block 0- 1=Ignore writes to block 0	0
2	EBI_nWE1	STRAP_NAND_FLASH	1=NAND	1
3	NAND_nRE	STRAP_EBI_ROM_SIZE1	0 = No ECC 1 = 1 BIT ECC 2 = 4 BIT ECC 3 = 8 BIT ECC	0
4	NAND_CLE	STRAP_EBI_ROM_SIZE0		0
5	NAND_ALE	Reserved	-	-
6	I2S_SDATA	STRAP_SYSTEM_BIG_ENDIAN	0 = Little endian- 1=Big endian	0
7	BCM_SPOIF_OUT	STRAP_RESET_EXT_MODE	1 = Extend initial Reset	0



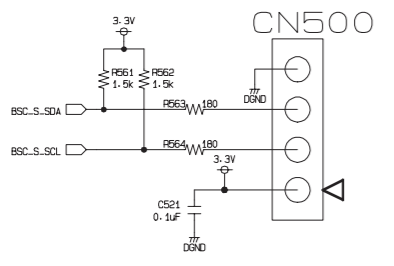
DDR STRAP OPTIONS

NO	SIGNAL NAME	VALUE
1	S_UART_TX0	1
2	IPOD_UART_TX1	0
3	UART_TX2	1
4	EPHY_LINK_GPI007	0

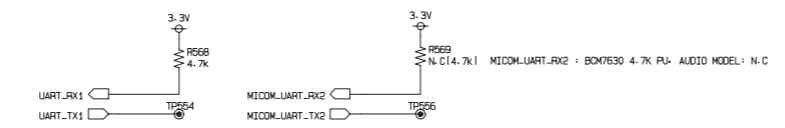
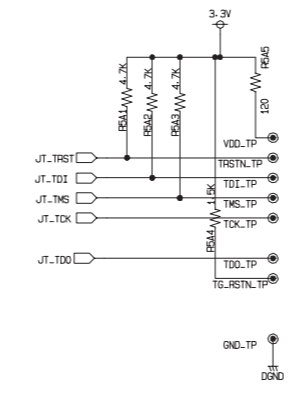
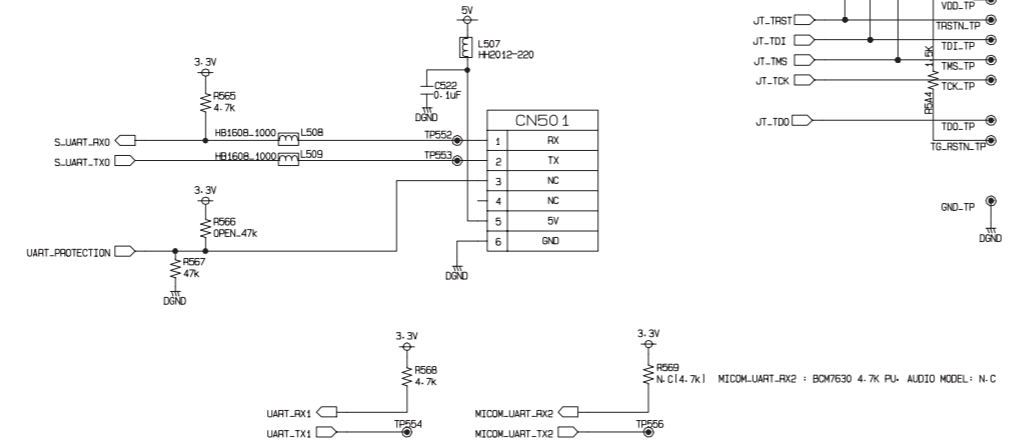
These configuration resistors do not need to be close to the BCM7630. So place them at the destination of the trace.



BBS I/F



DEBUGGING CONSOLE (UART1)



SCHEMATIC DIAGRAMS-5

5. MAIN - CPU 3 CIRCUIT

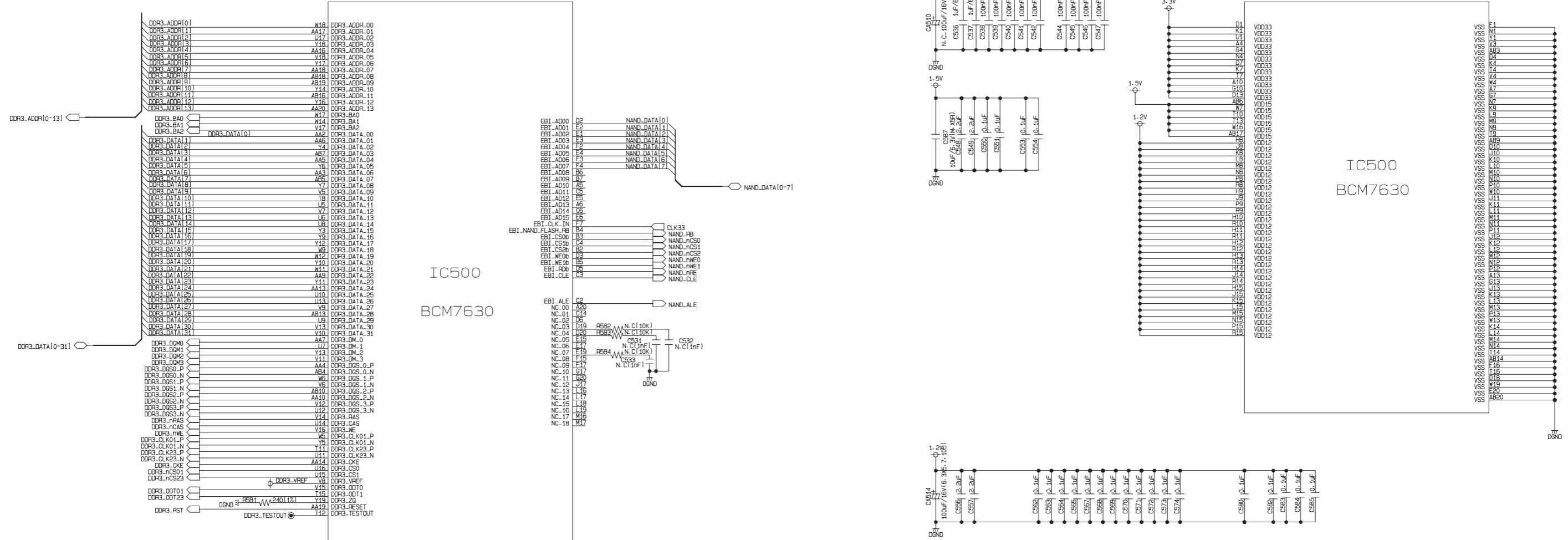
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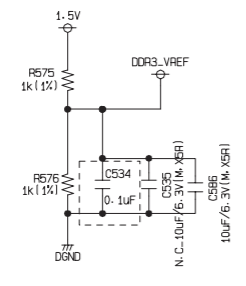
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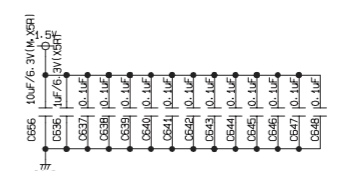
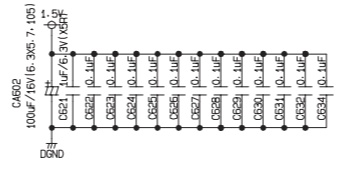
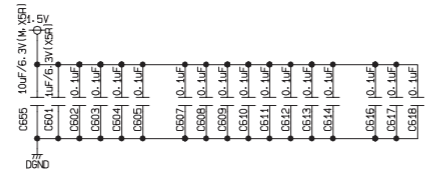


place C583 to V8 ball of 7630

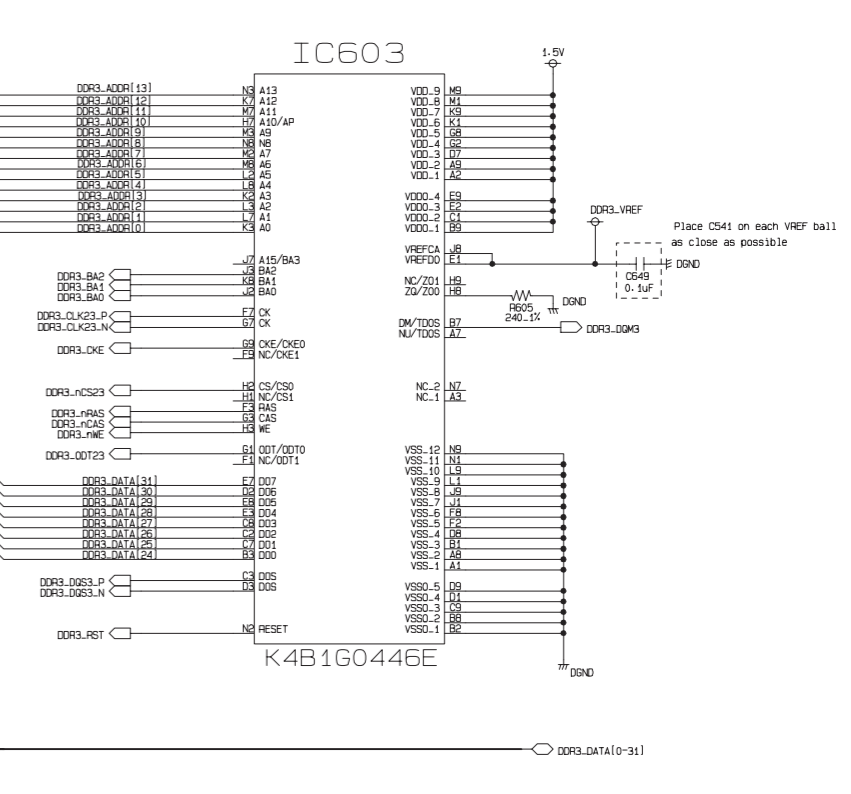
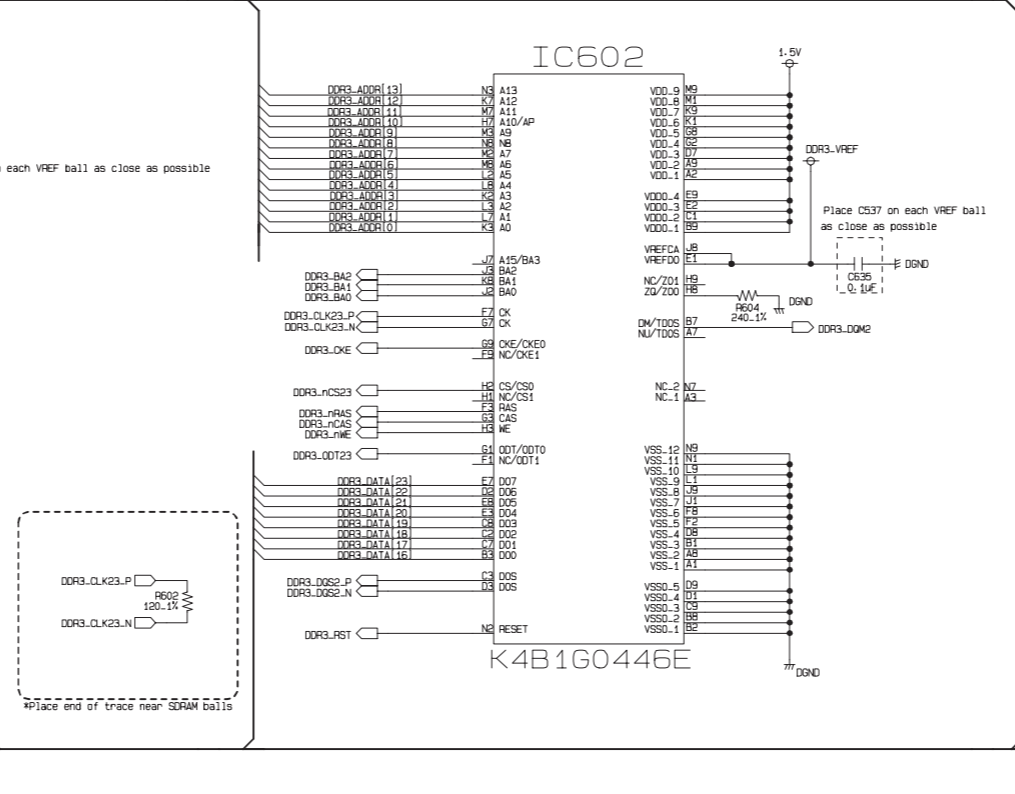
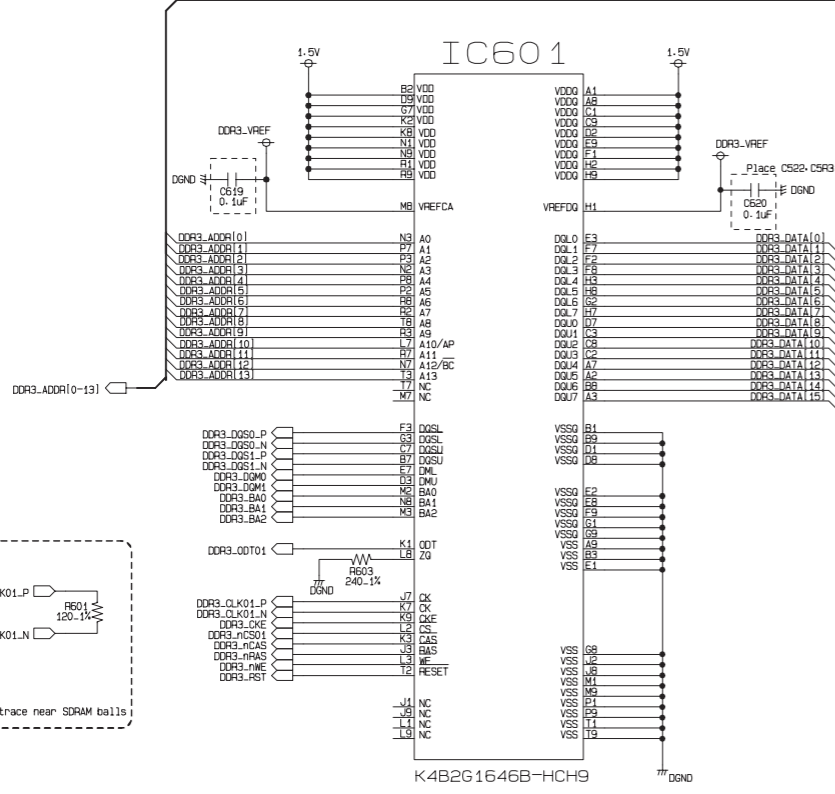


SCHEMATIC DIAGRAMS-6
6. MAIN - DDR2, NAND, CP CIRCUIT

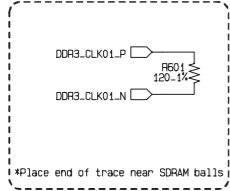
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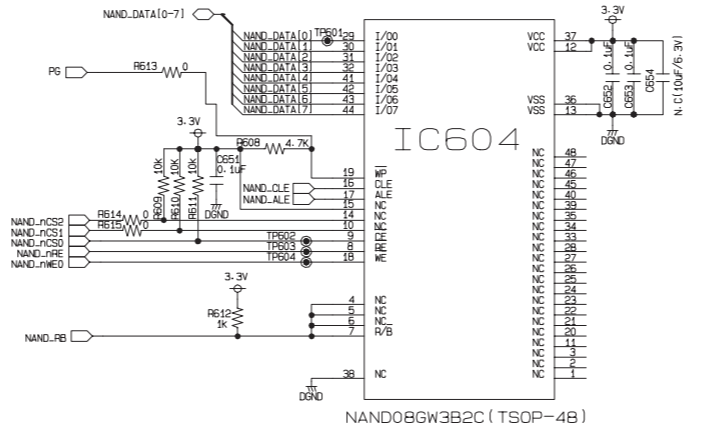
DDR3 SDRAM LAYOUT GUIDE

- * General Routing Guidelines**
 - Do not route critical signals across split planes.
 - Route over appropriate 1.5V or ground plane.
 - Avoid routing memory signals closer than 25-mil to the memory clocks.
 - DDR clock and DQS routed differentially (120ohm)
 - Use proper 120ohm clock termination
 - Vref decoupling close to DRAM
 - Vref decoupling close to ASIC
 - VDD/VDDQ decoupling close to DRAM VDD/VDDQ pins
 - VDDQ decoupling close to ASIC VDDQ pins
- * Clock Routing Guidelines**
 - Clocks must maintain length matching between clock pairs of 25 mils.
 - Differential clocks need to maintain length matching between positive and negative signals of 15 mils routed in parallel.
 - The space between differential pairs must be at least 2 the trace width of the differential pair to minimize loss and maximize interconnect density.
 - Match DQS signal length to related Clock signal length to within 475 mils
- * Address and Command Routing Guidelines**
 - Address and command signals are routed in a daisy chain topology from the first SDRAM to the last SDRAM.
 - Ensure that each net maintains the same consecutive order.
 - Do not route differential clock and clock enable signals close to address signals.
 - Route all addresses and commands to match related clock signals to within 475 mils to each discrete memory component.
 - (Values apply for two loads when both are near the end of the wire and the wire is not terminated. The Address/Control wire length to the first load should be longer than the clock wires.)
- * DQ-, DQS- and DM Routing Guidelines**
 - All signals within a given Byte Lane Group must be matched in length with a maximum deviation of 250mils.
 - Route all DQS-, DQM- signals to match related DQ byte lane signals to within 250 mils

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DDR3 : 512MB

SLC NAND : 256MB



NAND08GW3B2C (TSOP-48)

SCHEMATIC DIAGRAMS-7

7. MAIN - BCM7630 FRONT END CIRCUIT

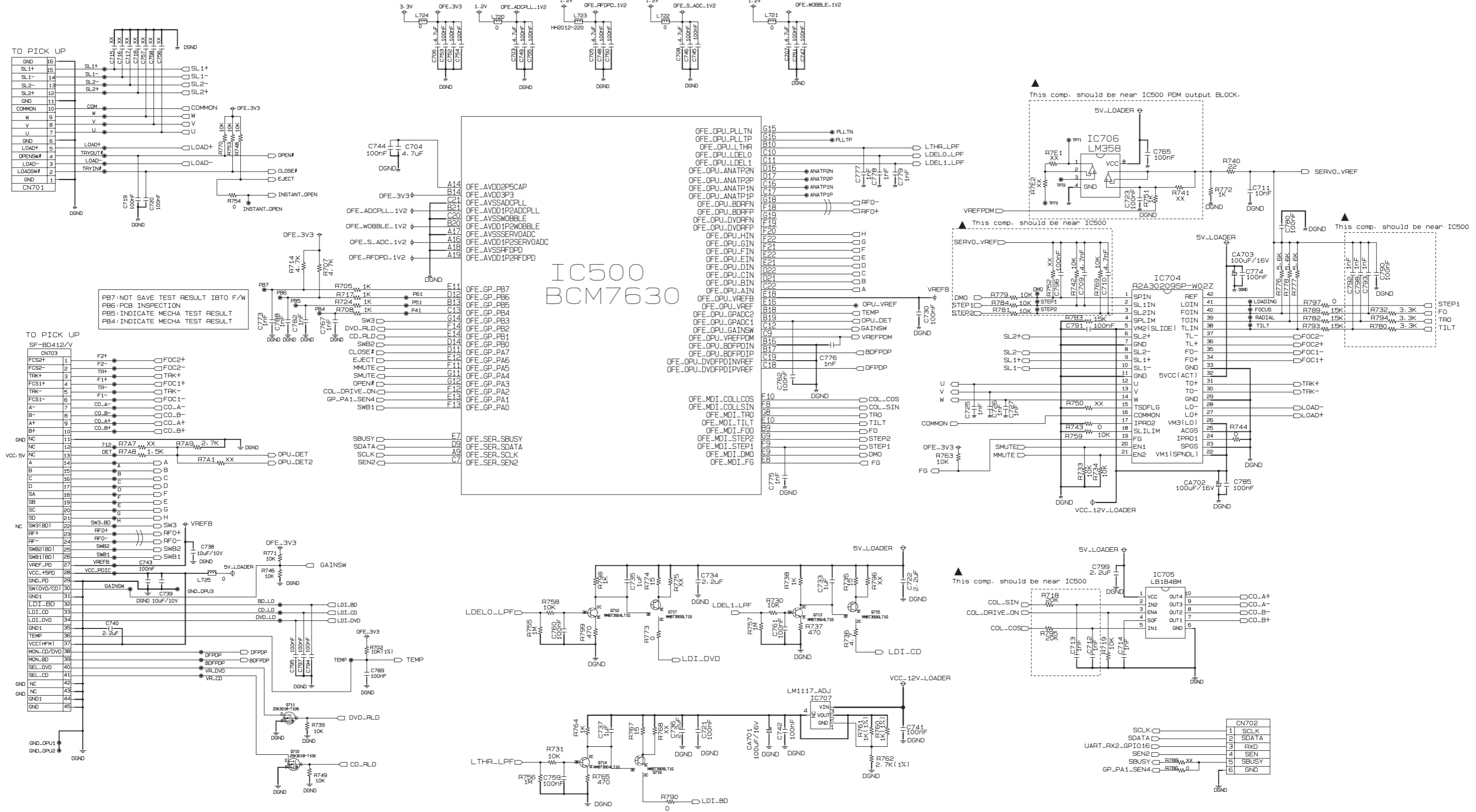
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PB7: NOT SAVE TEST RESULT IBTO F/W
 PB6: PCB INSPECTION
 PB5: INDICATE MECHA TEST RESULT
 PB4: INDICATE MECHA TEST RESULT

This comp. should be near IC500 PDM output BLOCK.

This comp. should be near IC500

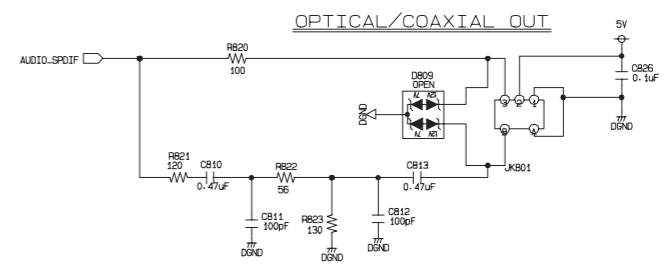
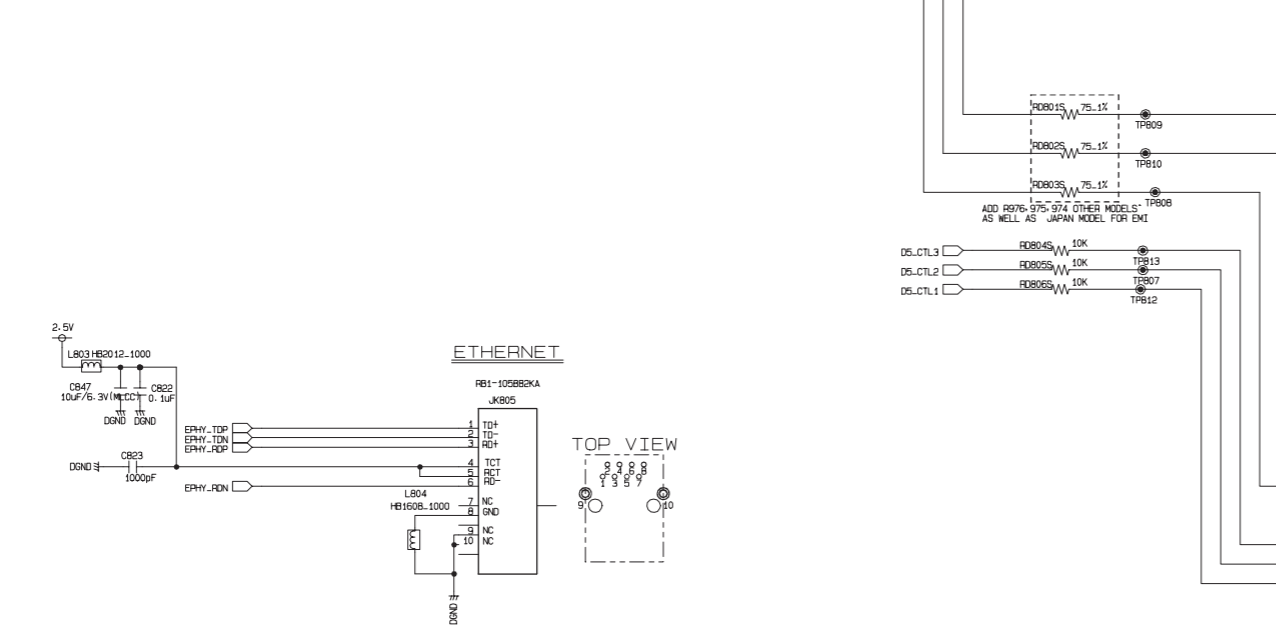
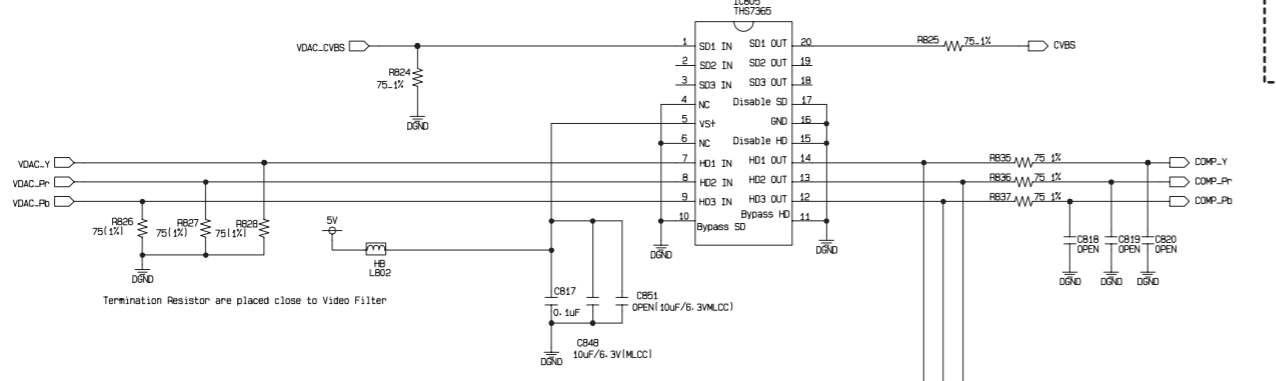
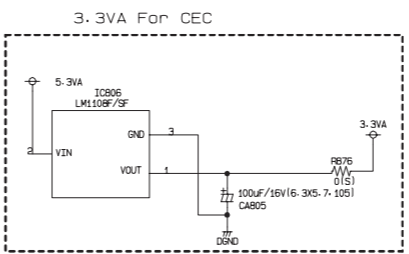
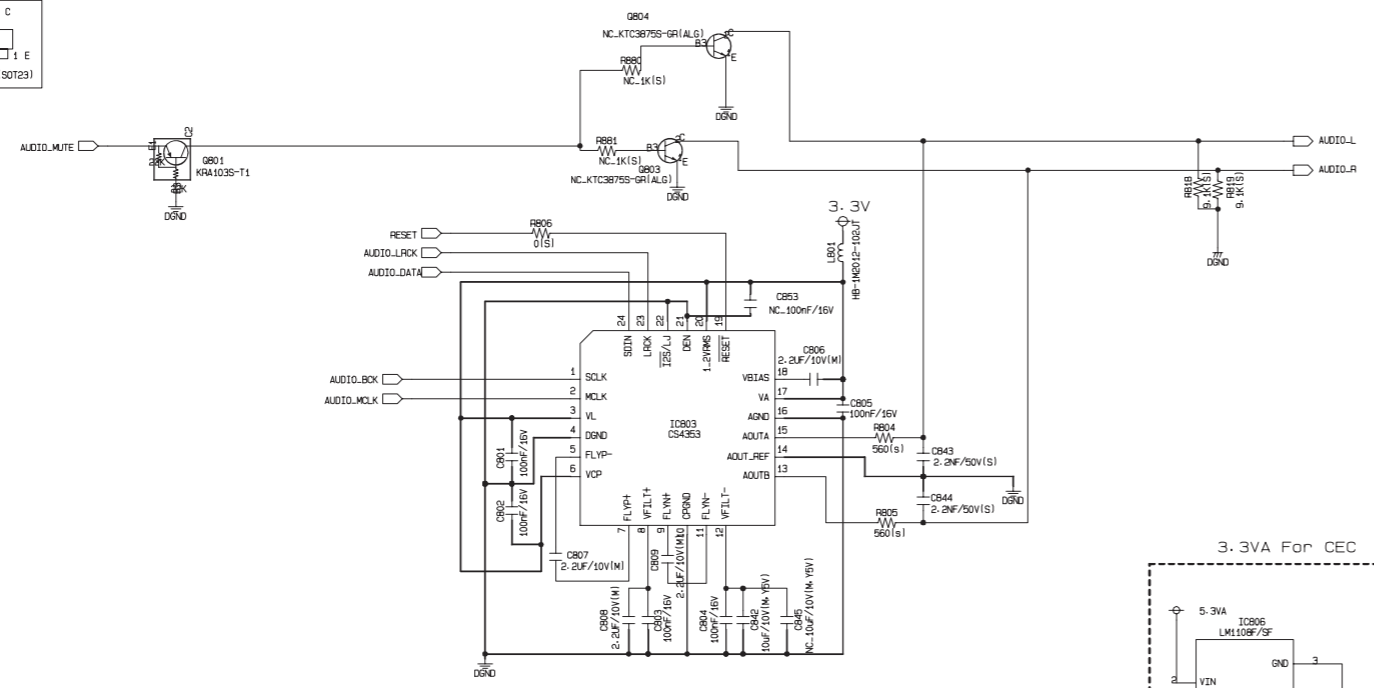
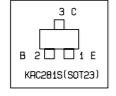
This comp. should be near IC500

This comp. should be near IC500

1	SCLK
2	SDATA
3	RXD
4	SEN
5	SBUSY
6	GND

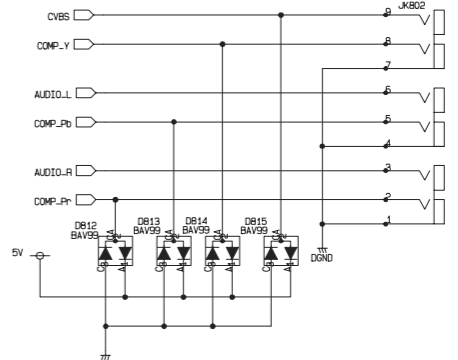
SCHEMATIC DIAGRAMS-8

8. MAIN - AUDIO/VIDEO OUTPUT CIRCUIT

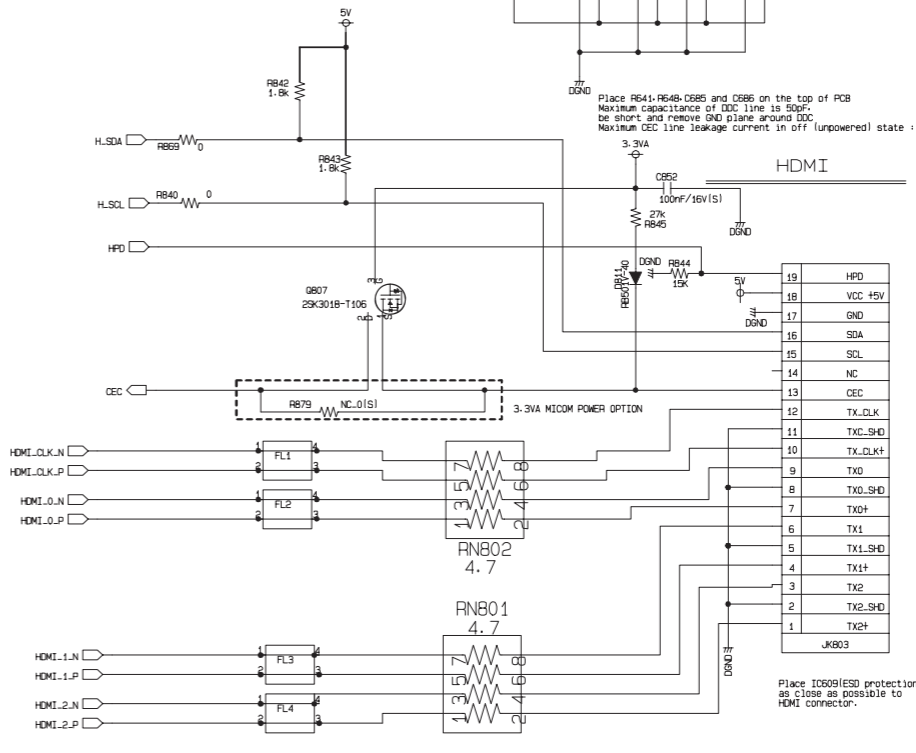


Audio & Video Signal Layout Guide
1.Component & CDS signal traces must be routed using signal to signal spacing is more than 0.25mm.

COMPONENT CVBS - 2CH AUDIO



Place RB41-RB48, CB85 and CB86 on the top of PCB
Maximum capacitance of DDC line is 50pF
be short and remove GND plane around DDC
Maximum CEC line leakage current in off (unpowered) state : 1.8



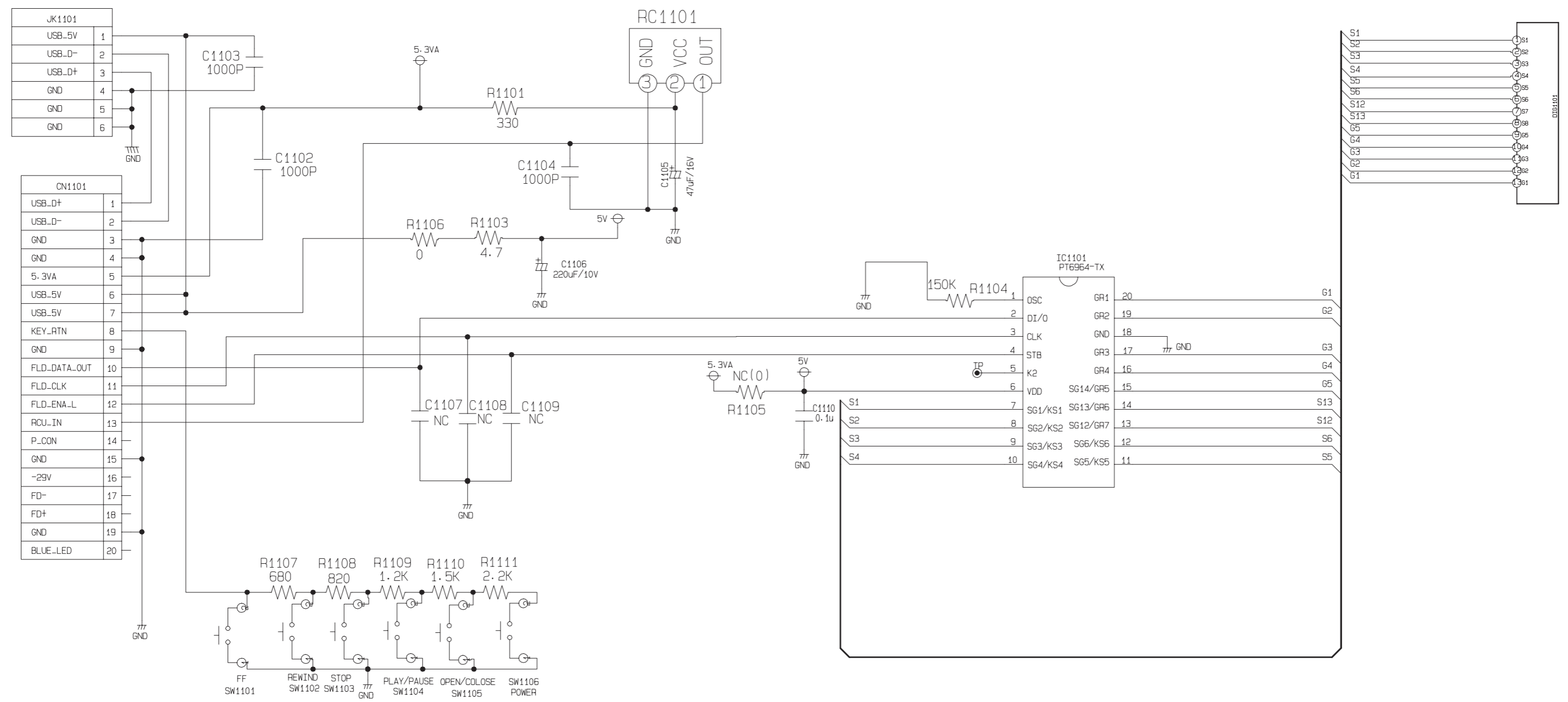
HDMI Design & Layout Guide
1.HDMI differential pair signals must be routed as 100ohm differential pairs.
2.Match trace length of differential pairs.
3.Trace spacing is same as trace width within pair signals.
4.Route differential pairs above gnd plane and gnd plane are not split under differential pairs.
5.Avoid via as possible as you can.
6.Trace spacing between DP/DN and other traces must be more than 5 times of DP/DN trace width.
7.Trace length must be less than 100mm.

SCHEMATIC DIAGRAMS-9

9. FRONT - TIMER CIRCUIT

9-1. TOOL TIMER CIRCUIT

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SCHEMATIC DIAGRAMS-10

9. FRONT - TIMER CIRCUIT

9-2. TOOL TIMER CIRCUIT

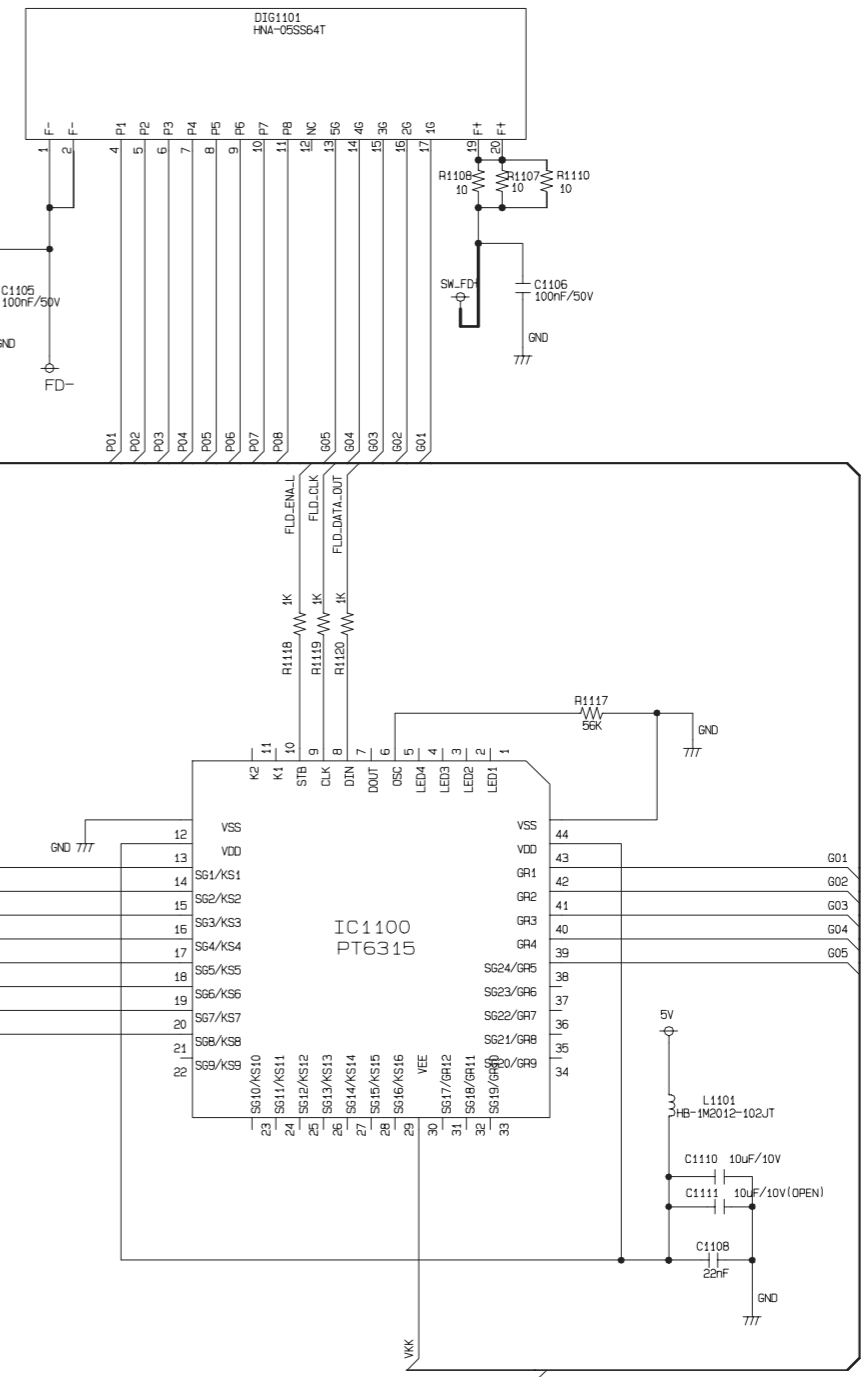
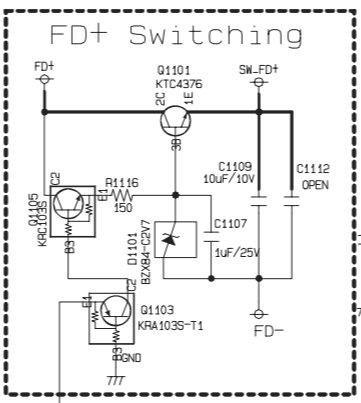
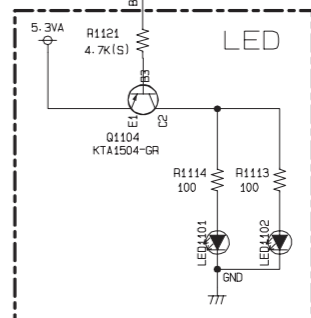
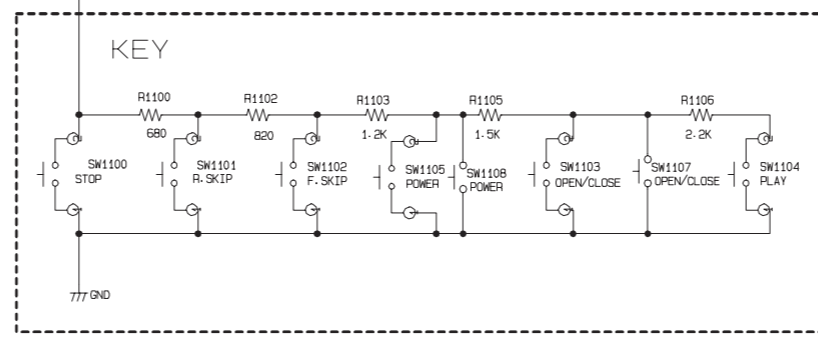
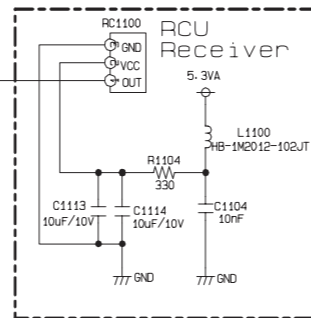
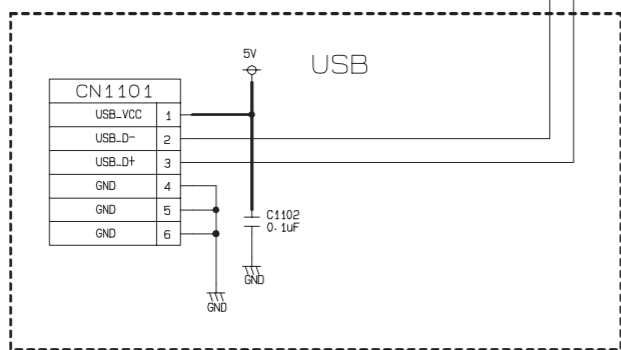
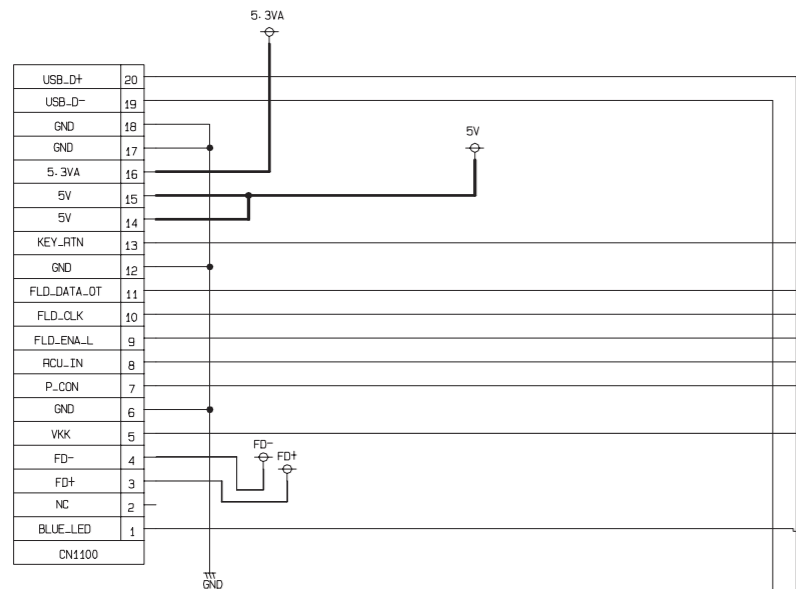
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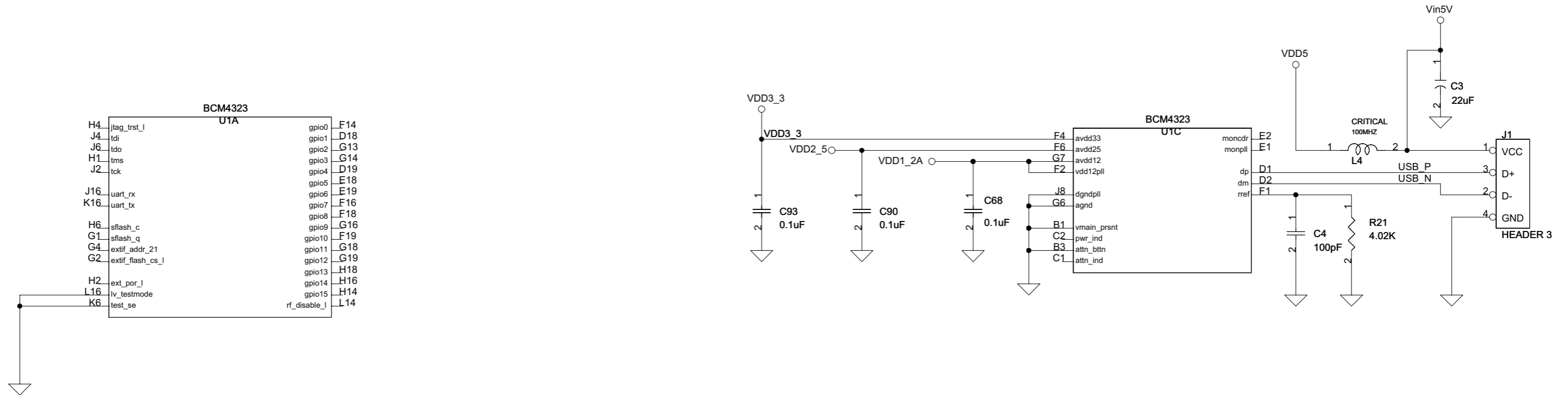
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SCHEMATIC DIAGRAMS-11
10. WiFi - USB GPIO STRAP CIRCUIT

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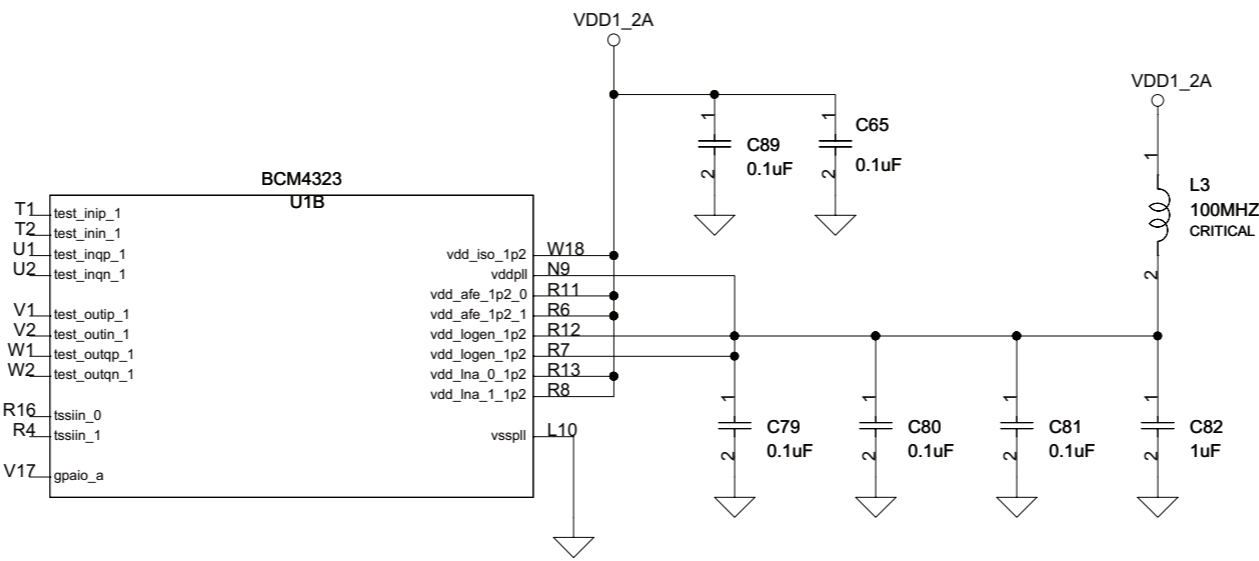
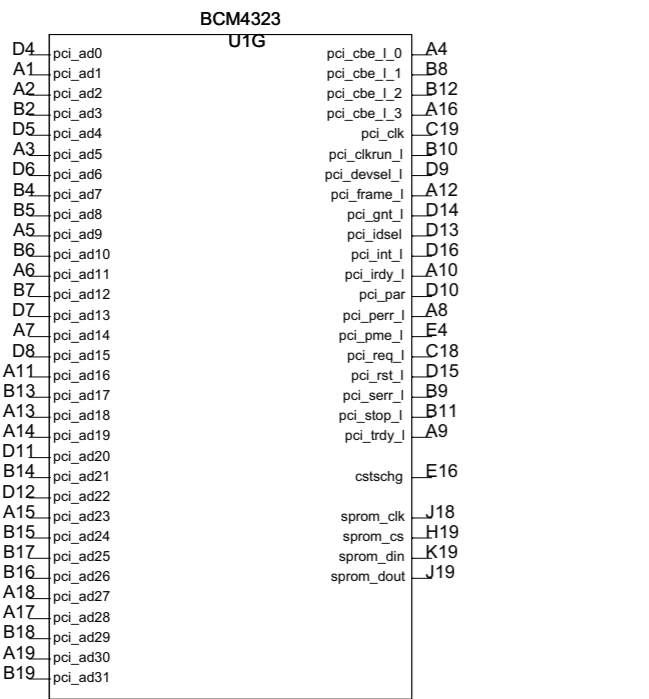


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Pin name	Netname	Status
mimophy_core1_ant2_swctrl_1	VRXA1_1	ext PD
mimophy_core1_ant1_swctrl_1	VRXA0_1	ext PU
mimophy_pa_cntrl_2g_1	PA_cntrl_2G_1	ext PU
mimophy_core0_ant1_swctrl_1	VRXA0_0	ext PU
mimophy_ext_lna_2g_pu_0	xlna_cntl_2g_pu0	ext PU
mimophy_core1_ant1_swctrl_2	VTXA0_1	ext PU

SCHEMATIC DIAGRAMS-12

11. WiFi - POWER & CONTROL CIRCUIT

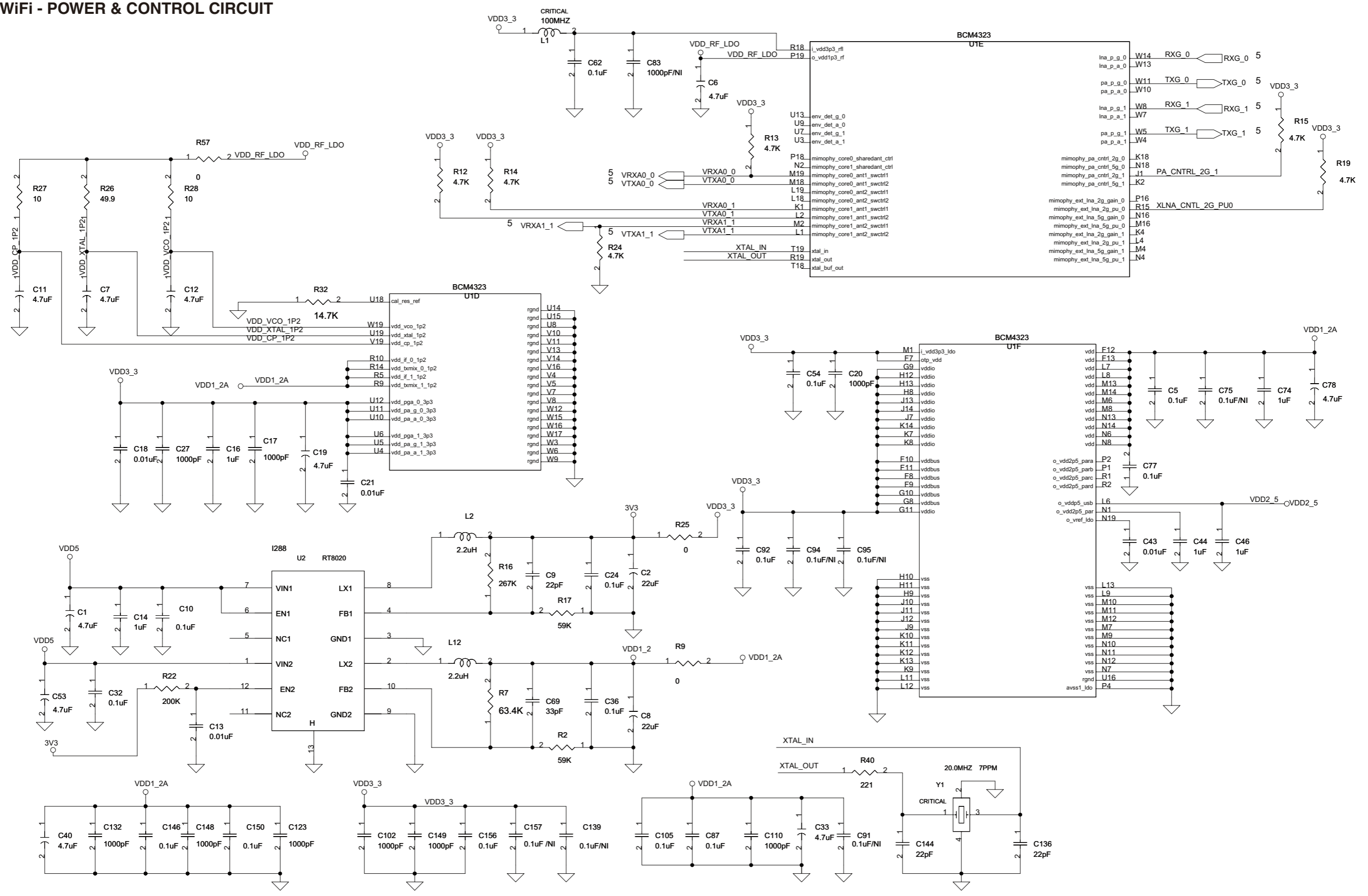
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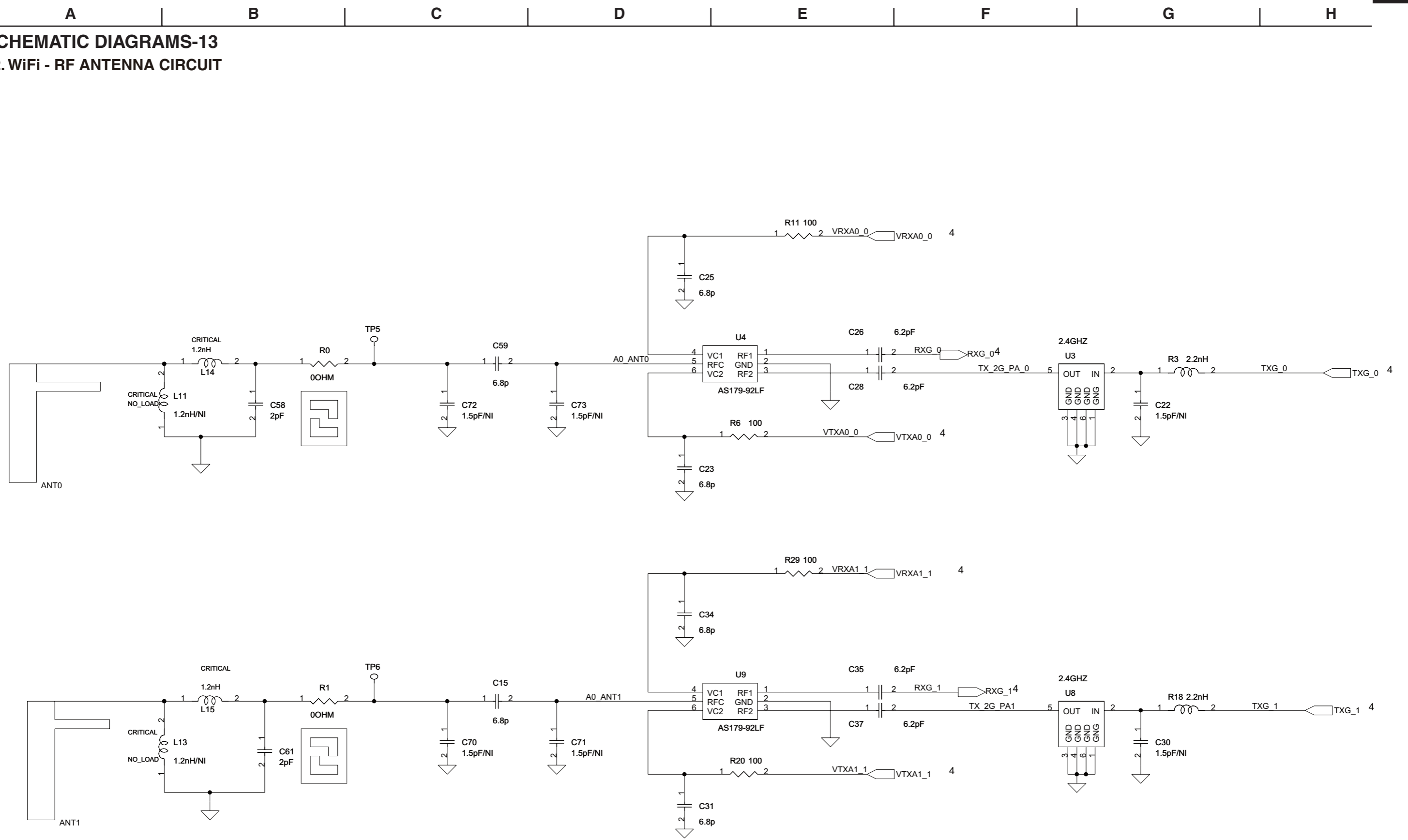
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SCHEMATIC DIAGRAMS-13
12. WiFi - RF ANTENNA CIRCUIT

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A B C D E F G H

SCHEMATIC DIAGRAMS-14

CIRCUIT VOLTAGE CHART

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1. MAIN BOARD - ICs

PIN NO.	DESCRIPTION	VOLTAGE	
		PLAY MODE	NO PLAY MODE
IC201(MP2377)			
1	Vout	1.22	1.22
8	Vin	12.47	12.35
IC202(MP8706)			
1	Vin	12.47	12.36
3	Vout	1.51	1.51
IC203(LM39102D)			
2	Vin	4.45	4.47
3	Vout	3.33	3.33
IC205(LM29152)			
2	Vin	5.35	5.36
4	Vout	5	5.01
IC206(LM29152)			
2	Vin	13.43	13.32
4	Vout	12.12	12.13
IC207(LM39102D)			
1	Vin	5.35	5.36
2	Vout	4.98	4.99
IC803(CS4353) DAC+AMP			
3	VL	3.329V	3.337V
6	VCP	3.329V	3.337V
18	VA	3.329V	3.337V
20	V_2VRMS	3.329V	3.337V
IC805 Video Amp			
5	VCC	5.07	
20	CVBS Out	1.64	

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2. MAIN BOARD - Capacitors

LOCA. NO.	CAPACITY	PLAY MODE		NO PLAY MODE	
		POSITIVE	NEGATIVE	POSITIVE	NEGATIVE
CA201	100uF/16V	4.98	0	4.98	0
CA202	100uF/16V	3.33	0	3.33	0
CA203	100uF/16V	5	0	5.01	0
CA239	100uF/16V	12.12	0	12.12	0
CA514	100uF/16V	1.21	0	1.21	0
CA602	100uF/16V	1.51	0	1.51	0
CA805	100uF/16V	3.3	0	3.3	0

3. FRONT BOARD

PIN NO.	DESCRIPTION	VOLTAGE
DIG1101(HNS-05SS64T)		
FD+	-	-18.9
FD-	-	-20.6
IC1100(PT6315) VFD Driver IC		
13, 43	VDD	4.99
30	VKK	-23.01
Q1101(KTC4375)		
Emitter	-	-18.9
Base	-	-18.01
Collector	-	-16.9
Q1105(KRC103S)		
Emitter	-	-16.86
Base	-	4.93
Collector	-	-16.89
Q1103(KRA103S)		
Emitter	-	4.96
Base	-	0
Collector	-	4.93
RC1100 RCU Receiver		
2	VCC	5.01

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